xLLM Technical Report

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Abstract

We introduce **xLLM**, an intelligent and efficient Large Language Model (LLM) inference framework designed for high-performance, large-scale enterprise-grade serving, with deep optimizations for diverse AI accelerators. Current mainstream inference frameworks face practical challenges. On the one hand, enterprise-grade serving struggles with hybrid and dynamic workloads, strict demand for high availability of services, and distributed storage management. On the other hand, inference execution is bottlenecked by underutilized AI accelerators due to new paradigms of hardwares, model architectures and inference algorithms.

To address these challenges, xLLM builds a novel decoupled service-engine architecture. At the service layer, xLLM-Service features an intelligent scheduling module that efficiently processes multimodal requests and co-locates online and offline tasks through unified elastic scheduling to maximize cluster utilization. This module also relies on a workload-adaptive dynamic Prefill-Decode (PD) disaggregation policy for instance scheduling and a novel Encode-Prefill-Decode (EPD) disaggregation policy designed for multimodal inputs. Furthermore, it incorporates a distributed architecture to provide global KV Cache management for efficient AI accelerator memory handling and robust fault-tolerant capabilities for high availability. At the engine layer, xLLM-Engine co-optimizes system and algorithm designs to fully saturate computing resources. This is achieved through comprehensive multi-layer execution pipeline optimizations, including overlapping CPU scheduling with AI accelerator operations to minimize computational bubbles, employing dual-stream parallelism to overlap computation with communication, and fine-grained overlapping of various computational units to maximize hardware utilization. These are complemented by an adaptive graph mode that drastically reduces kernel launch overhead, alongside the innovative "logically contiguous, physically discrete" xTensor memory management which resolves memory allocation conflicts. xLLM-Engine also further integrates algorithmic enhancements such as optimized speculative decoding and dynamic Expert Parallel Load Balance (EPLB), collectively serving to substantially boost throughput and inference efficiency.

Extensive evaluations demonstrate that xLLM delivers significantly superior performance and resource efficiency. Under identical TPOT constraints, xLLM achieves throughput up to 1.7× that of MindIE and 2.2× that of vLLM-Ascend with Qwen-series models, while maintaining an average throughput of 1.7× that of MindIE with Deepseek-series models. We have deployed xLLM in production to support a range of core business scenarios at JD.com, covering areas including LLM, Multimodal Large Language Model (MLLM), and generative recommendation. These applications encompass the JingYan AI chatbot, marketing recommendations, product understanding, customer service assistants, and more. xLLM framework is publicly available at https://github.com/jd-opensource/xllm and https://github.com/jd-opensource/xllm-service.

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1 Introduction

In recent years, large language models (LLMs) with parameters ranging from billions to trillions (GPT [1], Claude [2], DeepSeek [3], LLaMA [4], etc.) have achieved breakthrough progress in the fields of natural language processing and multimodal interaction, which drives an urgent demand in the industry for efficient inference engines and service systems. These models are being rapidly deployed in core business scenarios such as intelligent customer service [5], real-time recommendation [6], and content generation [7]. However, how to reduce the cost of model inference and improve computing efficiency remains a key challenge for large-scale commercial serving.

Current mainstream LLM inference frameworks (vLLM [8], SGLang [9], TensorRT-LLM [10], etc.) face four key challenges in enterprise-level serving scenarios: *First*, in an inference cluster with hybrid deployment, online inference requests exhibit significant tidal characteristics [11, 12]. Current scheduling systems fail to meet the service level objective (SLO) for online services while fully leveraging idle periods of online services to increase the throughput of offline tasks. *Second*, existing Prefill-Decode (PD) disaggregation architecture [13–15] assumes static resource allocation for the two phases, which cannot adapt to the dynamically changing request loads (i.e., input/output lengths fluctuate) in real-world applications, resulting in low AI accelerator utilization and increased SLO violation risks. *Third*, there is a lack of strategy to efficiently service multimodal requests (i.e., image, voice and text input [16, 17]), including parallel processing for the encode phase and fine-grained resource allocation accordingly. *Fourth*, as the scale of the inference cluster increases, ensuring fast fault detection and service recovery for nodes or instances is critical to maintaining the stability of inference services.

The evolving computing paradigms also present significant performance challenges on existing LLM inference engines: *First*, they struggle to fully utilize the computing units of modern AI accelerators [18, 19]. *Second*, the All-to-All communication overhead [20] and expert parallel (EP) load imbalance in the Mixture of Experts (MoE) architecture [21, 22] restrict the scalability of the system. *Third*, as the model context window continues to expand, efficient KV Cache management becomes critical to inference performance [23]. *Forth*, Due to the unpredictable nature of inference requests, conventional static scheduling and operator strategies face difficulties in effectively balancing workloads across computing units in Data Parallelism (DP).

To address above challenges , we propose **xLLM**, an efficient and intelligent LLM inference framework featuring a service-engine decoupled design. xLLM achieves efficient support for enterprise-level inference through the following innovations: at the *service layer*, xLLM has made groundbreaking achievements in 1) unified elastic scheduling for online/offline requests, 2) workload-adaptive dynamic PD disaggregated architecture, 3) novel Encode-Prefill-Decode (EPD) disaggregation for multimodal requests, and 4) a distributed cache management and fault-tolerance framework; at the *engine layer*, xLLM enhances the resource efficiency across the full-stack of "communication-computation-storage", including 1) a multi-layer pipeline execution mechanism, 2) efficient computing and memory optimization, and 3) intelligent algorithm designs.

Specifically, **xLLM-Service** schedules online requests with preemptive execution and offline requests in a best effort manner, to maximize resource utilization while strictly ensuring SLOs for online services. To address the inherent limitations of the static PD configuration, xLLM incorporates an adaptive scheduler to dynamically adjust the proportion of PD instances for each request and supports fast role reversal for instances, by monitoring key metrics such as Time to First Token (TTFT) and Time Per Output Token (TPOT) [24]. For multimodal visual requests, xLLM automatically selects the optimal EPD phase-disaggregation strategy based on pre-profiling, for the best performance trade-off between throughput and latency. To handle failures such as hardware problems, network faults, or software errors [25], xLLM collects node error information, evaluates KV recomputation or migration costs of interrupted requests, and makes optimal global rescheduling decisions. Across multiple instances, xLLM supports KV offloading and routing migration within a hybrid storage architecture, improving KV storage capacity and cache hit rates.

xLLM-Engine employs a multi-layer execution pipeline that incorporates hardware-specific optimizations: (i) at the framework scheduling layer, it implements asynchronous CPU-accelerator scheduling to minimize computational idle time; (ii) at the model graph layer, it utilizes dual-stream micro-batch parallelism to overlap computation with communication; (iii) at the operator level, it achieves kernel computation and memory access overlapping. For computational efficiency, xLLM-

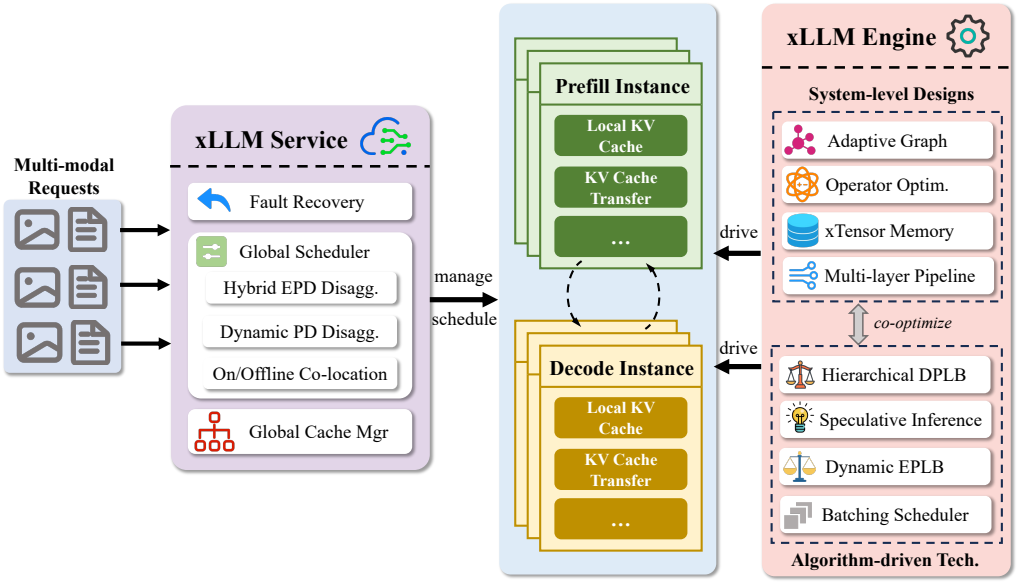

Figure 1: Overview of xLLM's capabilities, with decoupled service-engine architecture.

Engine automatically fuses small kernels into a unified computation graph and dispatches them to the accelerator in a single operation, significantly reducing kernel launch overhead. Regarding memory management efficiency, xLLM-Engine introduces the xTensor memory management scheme, which employs a "logically contiguous, physically discrete"" KV cache storage structure that resolves the conflict between memory contiguity requirements and dynamic allocation needs. To further enhance performance, xLLM-Engine incorporates an adaptive speculative decoding mechanism, a redundant expert-based load balancing algorithm for EP, and a hierarchical load balancing algorithm for DP. Additionally, xLLM-Engine provides scenario-specific optimizations, such as for generative recommendation – one of JD.com's core businesses – where it achieves 23% performance improvement through host-kernel operation overlapping.

In summary, we make the following contributions when developing xLLM:

xLLM Intelligent Service Capabilities

- We design a unified scheduling algorithm for online/offline workloads (§3.1).
- We implement a workload-adaptive PD disaggregation policy to address scenarios with rapidly changing traffic load and request input/output lengths (§3.2).
- We propose a hybrid EPD disaggregation policy for multimodal requests, achieving intelligent resource allocation across different phases (§3.3).
- We leverage multi-level KV Cache management and global KV Cache routing strategy to expand KV Cache capacity and improve cache hit rates (§3.4).
- We design a multi-node fault tolerance architecture to ensure high service availability (§3.5).

xLLM Intelligent Engine Capabilities

- We achieve intelligent and efficient inference, through hardware-software co-design to improve hardware computing efficiency, including pipeline execution (§4.1), graph optimization (§4.2), and memory optimization (§4.3).
- We enhance inference performance through algorithmic optimizations (§4.4), including optimized speculative decoding (§4.4.1), dynamic expert parallel load balance (§4.4.2), and hierarchical data parallel load balance (§4.4.3).
- We optimize online inference for generative recommendation scenarios (§4.5).

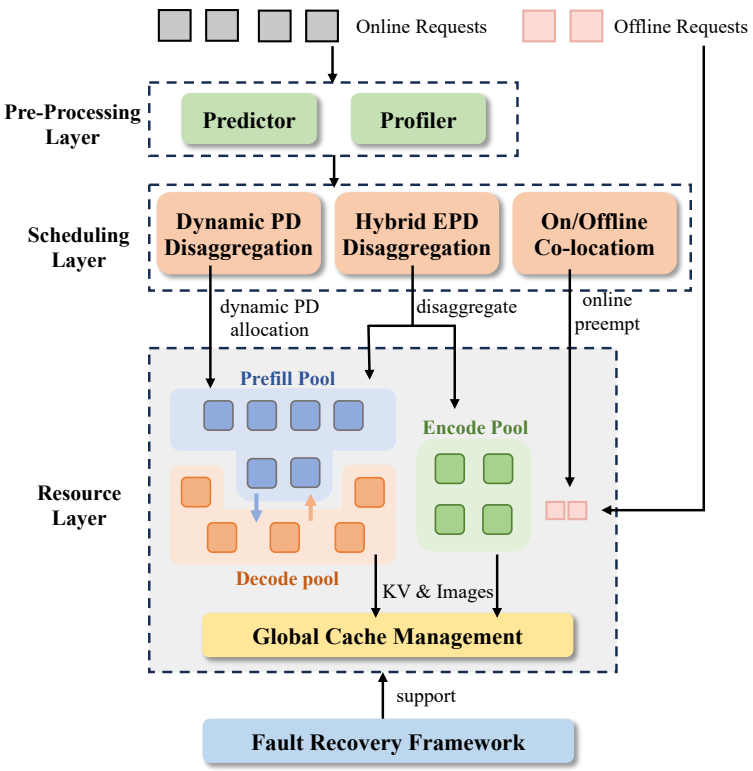

Figure 2: System workflow of xLLM-Service.

2 System Overview

The overall architecture of xLLM is depicted in Figure 1. Upon request arrival, xLLM-Service performs intelligent scheduling to distribute each request to one of three elastic instance pools and manages instance migration across these pools during runtime. xLLM-Engine then drives efficient request inference by orchestrating system- and algorithm-level optimizations.

2.1 xLLM-Service

We describe the workflow of xLLM-Service in Figure 2. The system comprises three primary layers: 1) a preprocessing layer consisting predictor and profiler, 2) a scheduling layer integrating three policies (*Dynamic PD Disaggregation Policy*, *Hybrid EPD Disaggregation Policy*, and *Online-Offline Co-location Policy*), and 3) a resource layer consisting of three heterogeneous instance pools. Specifically, the *Dynamic PD Disaggregation Policy* leverages information from the predictor to dynamically convert PD instances based on the workload status of the two instance types. The *Hybrid EPD Disaggregation Policy* utilizes the profiler to determine the optimal EPD disaggregation strategy for multimodal requests. Concurrently, the *Online-Offline Co-location Policy* dispatches requests according to their online or offline attributes. KV and image caches are offloaded and routed among distributed instances, while the fault recovery framework ensures the high availability of the entire service.

Elastic Instance Pools. Instances in a cluster are partitioned into three elastic pools:

- ▷ Prefill Instance Pool: This pool handles the prefill phase of text requests.
- ▷ Decode Instance Pool: This pool handles the decode phase of text requests.
- ▷ Encode Instance Pool: This pool handles the encode phase of multimodal requests.

We design the instances in Prefill and Decode pools as stateless, i.e., instances do not require physical migration between instance pools. Instead, they achieve flexible switching between Prefill-Decode roles based on the type of request being processed.

Request Preprocessing. xLLM-Service implements unified resource management for both online and offline requests. Online requests are submitted in a preemptive and deadline-prioritized manner, and are co-deployed with best-effort offline tasks within the shared resource pool. During the runtime of an offline request, the *Unified-Scheduler* dynamically scales it up/down based on the tidal traffic characteristics of online requests. When an online request is submitted, it first passes through the pre-processing layer, which consists of two modules:

▷ TTFT Predictor: A TTFT prediction model built for text requests. It evaluates SLO fulfillment by analyzing queueing delays from each prefill instance queue and request input lengths, thereby guiding instance allocation for the *Dynamic PD Disaggregation Policy* in the scheduling layer.

▷ EPD Profiler: A profiler for multimodal requests that uses binary search to identify optimal deployment configurations: (1) EPD separation strategy, choosing from three approaches: EP-D (i.e., aggregated execution of Encode and Prefill phases, with Decode phase executed separately), ED-P, or E-P-D; (2) The maximum batch size for the Encoder phase; (3) The maximum number of tokens for Prefill/Decode's inputs. The *Hybrid EPD Disaggregation Policy* in the scheduling layer will use the optimal configuration determined for phase disaggregation and task dispatching.

Intelligent Scheduling. The intelligent scheduling layer adjusts resource allocation for requests across their full lifecycles. It contains three major scheduling policies designed for various scenarios:

▷ Online-Offline Co-location Policy: This policy implements a preemptive scheduler for managing online and offline requests. When the load of online requests reaches the peak, they preempt some offline requests on PD instances. To surrender resources to offline requests, when the load on P instances decreases (usually earlier than on D instances), P instances continue to process offline prefill requests and also migrate decode offline requests from D instances to P instances.

▷ Dynamic PD Disaggregation Policy: This adaptive scheduling policy is responsible for dynamically managing P and D instance allocation. It intelligently assigns requests to suitable instances using a heuristic algorithm guided by the TTFT Predictor. Furthermore, it implements a feedback mechanism by continuously collecting performance data from computing instances, enabling runtime monitoring and adjustment of allocation decisions to maintain system efficiency.

▷ Hybrid EPD Disaggregation Policy: This multimodal policy executes the three-phase disaggregation based on strategies searched by the EPD Profiler. For the EP-D disaggregation, the fused EP phase executes in the P instance pool; for the ED-P disaggregation, the fused ED phase executes in the D instance pool; for the E-P-D disaggregation, the three phases execute separately in the three instance pools. This deployment also enables multimodal requests to benefit from the adjustment of *Dynamic PD Disaggregation Policy*.

KV-centric Storage Architecture. The instance storage employs a hybrid architecture (HBM-DRAM-SSD) to cache KV values and image tokens. At the global level, xLLM takes the idea from Mooncake Store [23] and extends it to domestic accelerators with specific optimizations. Routing and reuse of caches across instances are determined by embedded intelligent routing strategies.

Efficient Fault-tolerant. The fault recovery framework of xLLM-Service supports fault detection and fast recovery of instances from the three elastic pools (E, P, D). For requests on failed instances, the architecture manages the migration of image caches between instances, and automatically decides the optimal KV recomputation or migration strategy for handling affected KV caches.

2.2 xLLM-Engine

During request execution, the xLLM-Engine layer provides intelligent computing capabilities. We achieve various joint inference accelerations between the computing system layer and the algorithm-driven layer in the following ways:

Computing System Layer

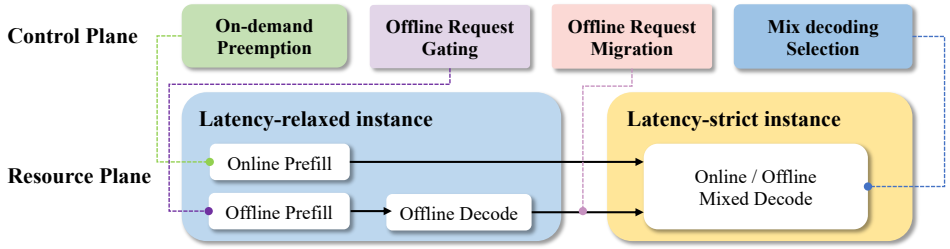

Figure 3: Overview design of Online-Offline Co-location Scheduler Policy.

▷ Multi-layer Pipeline Execution Engine: In the framework layer, CPU tasks are scheduled asynchronously to create a pipeline with inference computation, reducing computational bubbles; in the model graph layer, a single batch is split to form a pipeline between two micro-batches, effectively overlapping computation and communication; in the operator kernel layer, operations are pipelined across different computational units, enabling computation and memory access to overlap.

▷ Graph Optimization for Dynamic Inputs: Small kernels in the decoding stage are fused into a single computational graph. To handle variable sequence lengths and batch sizes, we parameterize the input dimensions, and employ a multi-graph caching scheme to reduce compilation overhead.

▷ xTensor Memory Management: It uses a "logically continuous, physically discrete" KV storage structure. It allocates physical memory space on-demand during token generation for each request, while asynchronously predicting and intelligently mapping the physical pages required for the next token. When a request completes, the existing physical memory will be reused to execute the next request.

Algorithm-Driven Layer

▷ Speculative Decoding: xLLM-Engine incorporates an optimized speculative inference algorithm that generates multiple tokens at once to boost throughput [26]. It further optimizes the computing architecture through ways like asynchronous CPU processing and reduced data transfer.

▷ EP Load Balance: For MoE models, xLLM implements expert weight updates based on historical expert load statistics, enabling effective dynamic load balancing during inference.

▷ DP Load Balance: For data parallel (DP) deployment, xLLM achieves fine-grained load balance by kvcache-aware instance allocation, inter-DP requests migration, and intra-DP computing units allocation.

We will elaborate on the detailed design of xLLM-Service in §3 and outline the optimizations within the xLLM-Engine in §4. A comprehensive evaluation of xLLM will be presented in §5.

3 xLLM-Service Designs

3.1 Online-Offline Co-location Scheduler Policy

Online/Offline Request Characteristic. LLM services can be categorized into two types based on their service modes: online and offline requests. Online requests, including those from chatbots [1, 2, 27], code completion [28–30], and recommendation systems [31, 32], constitute latency-sensitive workloads. These services must respond immediately upon request arrival, often returning each generated token in real time via streaming output. Consequently, they impose strict SLO requirements on TTFT or TPOT to ensure a satisfactory user experience. In contrast, offline services, such as document analysis [33] and intelligent data annotation [34], are non-real-time workloads with minimal latency constraints and thus no stringent SLO requirements.

Furthermore, we observe that the request traffic for online services typically exhibits significant volatility, including tidal variations at hourly or daily scales and sudden bursts at minute-level intervals [11, 12]. While cluster auto-scaling [35] could theoretically mitigate resource underutilization caused by tidal patterns, the slow cold-start latency of instances—involving model loading and com-

plex initialization—renders it ineffective for responding to rapid traffic spikes [36], increasing the risk of service-level agreement violations.

Online/Offline Request Co-location Deployment. To address these practical challenges, we adopt a hybrid deployment strategy that co-locates online and offline requests. In such a system, offline requests can utilize idle resources during off-peak periods of online traffic. Conversely, during online traffic peaks, offline tasks can be preempted, as they are not bound by strict SLOs. This approach significantly enhances aggregate resource utilization and mitigates idleness during traffic troughs. Although some recent work [37–39] also attempts to co-locate offline requests, they have not explored the multi-instance scenario, especially for PD disaggregation.

Actually, the PD disaggregation architecture has demonstrated superior latency performance and is increasingly becoming a mainstream design paradigm in industry [13, 23]. However, directly applying online-offline co-location to PD-disaggregated systems introduces critical PD load imbalance issues: (1) such systems require the load ratio between prefill and decoding stages to align with their respective resource allocation ratios; otherwise, one stage may become a bottleneck, causing blocking or resource underutilization in the other. (2) Furthermore, as these PD load variations exhibit high volatility and burstiness similar to online traffic patterns, existing PD disaggregation techniques struggle to effectively address this challenge.

Latency-Constrained Decoupled Architecture. We rethink the design of PD disaggregation architecture under online-offline co-location deployment. The latency advantage of PD disaggregation essentially stems from the separation of latency constraints: the decoding phase is highly sensitive to per-step latency and cannot be blocked by long-duration operations, thus necessitating decoupling from the prefill phase. Inspired by this insight, we propose a latency-constrained decoupled architecture, as illstrated in Figure 3. This design regards cluster resources as two pools: a *latency-relaxed* pool (corresponding to original Prefill instances) and a *latency-strict* pool (corresponding to original Decode instances). All tasks are then reassigned to one of the two resource pools based on their inherent latency characteristics and requirements. Within this architecture, the decoding phase of offline requests can be executed in either resource pool. This flexibility allows us to dynamically adjust the load ratio between the two pools, thereby maximizing the overall resource utilization of the cluster.

However, it also introduces another two challenges: (1) Complex Scheduling Space: since the decoding of offline requests can be performed on either type of instance, how to leverage this flexibility to design new intelligent scheduling remains unknown. (2) Strict SLO Guarantee: the execution of offline requests consumes resources, their prefill phase may block newly arrived online requests, and their decode phase on *latency-strict* nodes may slow down the overall response speed. Both scenarios can compromise the SLO satisfaction of online requests.

Solution 1 - Performance Bottleneck Analysis. We construct an LLM inference performance model based on the Roofline Model [40] and online factor learning. This model is designed to predict the latency, computation utilization, and memory utilization of both the prefill and decode phases. Since decoding operations executed on *latency-strict* instances typically account for a large proportion of workloads and are highly performance-sensitive, we set balancing computational and memory resources as the optimization objective. By analyzing performance bottlenecks through this model, we can select more appropriate offline requests to merge into decoding batches, thereby improving resource utilization efficiency.

Solution 2 - Efficient Preemption Mechanism. To strictly ensure that the SLO of online requests remains unaffected, we introduce a preemption mechanism that allows online requests to preempt offline requests. For offline prefill tasks running on *latency-relax* nodes, we propose a model execution interruption technique, which enables preemption within an acceptable latency range without incurring additional model maintenance overhead. For decoding tasks running on *latency-strict* nodes, we leverage the performance model to dynamically select requests for decoding batching, ensuring that decoding latency always meets SLO constraints.

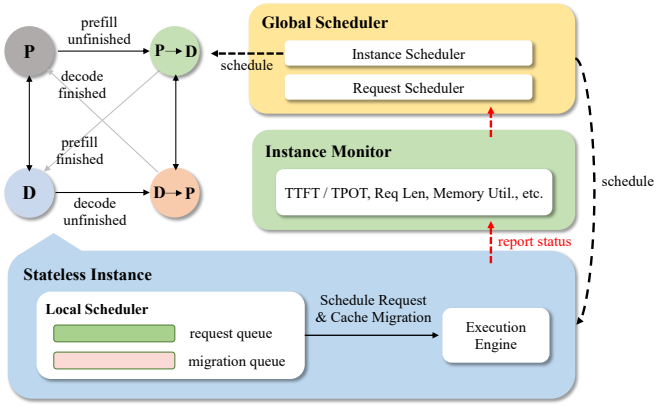

Figure 4: Overview design of Dynamic PD Disaggregation Scheduler Policy.

3.2 Dynamic PD Disaggregation Scheduler Policy

Inefficiency of Existing PD Disaggregation Policy under Workload Fluctuations. The Prefill-Decode (PD) disaggregated inference architecture [13, 24, 23, 41] partitions computing instances into dedicated prefill and decode instances, each handling their respective processing phases. This design mitigates interference between prefill and decode requests, achieving superior performance compared to PD co-located architectures [13].

However, we observe that most existing PD disaggregated systems employing static instance partitioning schemes suffer from low hardware utilization and inadequate responsiveness to traffic bursts. On one hand, existing analysis-based methods [13, 24, 23, 41] typically determine the PD ratio using profiling or simulator data. These approaches remain effective only when request arrival patterns and length distributions remain relatively stable. Under significant workload fluctuations, pre-collected analysis data often fails to accurately capture real-time request characteristics, leading to mismatches between preset load-balancing ratios and actual load requirements. On the other hand, when confronting substantial variations in input/output lengths within production workloads, existing PD disaggregation architectures [13, 42] generally adopt dynamic instance type adjustment strategies [43]. Nevertheless, online switching between prefill and decode instances typically involves multiple steps—including monitoring, waiting for flip conditions, and instance restarting—which introduces substantial latency overhead [15]. To address these limitations, we propose a Dynamic PD Disaggregation Policy that adaptively adjusts resource allocation in response to real-time workload characteristics.

Runtime Instance Monitor. Performance indicators such as TTFT and TPOT directly reflect the capability of instances to process requests in the prefill and decode phases, respectively. They serve as the core basis for evaluating whether an inference system can meet SLO requirements. Ideally, prediction-based methods could be adopted to dynamically assess these indicators. However, while TTFT exhibits relatively predictable characteristics (as its computation time is proportional to the square of the input sequence length [44, 41]), due to the uncertainty in the length of output tokens and transfer overhead, TPOT is difficult to accurately predict using traditional input/output features and cluster load metrics. To address this issue, we deploy additional instance monitors to collect real-time performance data from each computing instance. This data includes metrics such as the number and length of prefill and decode requests, memory usage, TTFT, TPOT, and token generation intervals. The system can further use these real-time performance indicators to dynamically evaluate instance loads and adjust scheduling strategies.

Stateless Instance and Elastic Pool. As illustrated in Figure 3, Dynamic PD Disaggregation Policy adopts a design of stateless instances and elastic instance pools to enable fast and dynamic switching of instance roles. First, it treats prefill or decode phase as the request attribute rather than instance attribute. Instances are designed to be stateless, allowing each instance to process both prefill and decode requests simultaneously. Additionally, to facilitate the management of multiple instances, we further extend PD pools to four elastic instance pools (i.e., P, D, P→D, D→P) as de-

scribed in §2.1. When flipping an instance (switching its role), we only needs to remove the instance from its original pool and move it to the new pool. This achieves zero-wait-time instance scheduling, avoiding the overhead of instance restart or model reloading incurred in traditional systems.

SLO-aware Instance Role Switching. The instance scheduling strategy is dynamically adjusted strictly based on SLO objectives: during the prefill phase, if it is predicted that existing instances cannot meet the TTFT requirements, the conversion of decode instances is triggered; while during the decode phase, when resource shortage occurs, the average token generation interval exceeds the TPOT threshold, or prefill instances are idle, the conversion of prefill instances to decode instances will be initiated to cope with sudden traffic surges. Specifically, when decode instances are reallocated to prefill instances, the scheduler prioritizes selecting the instance with the lightest load (i.e., the fewest tokens being processed) from the P→D pool for role conversion, and always ensures that at least two decode instances are available; conversely, when prefill instances are reallocated to decode instances, the scheduler prioritizes scheduling from the D→P pool, which avoids local overload and maximizes resource utilization.

SLO-aware Request Scheduling. The request scheduling scheme adopts a two-level architecture:

▷ Global Request Scheduler: The scheduler implements a greedy strategy of prioritizing the lightest load, while being strictly restricted by SLO constraints. For prefill requests, the scheduler first evaluates the estimated queuing latency of each instance in the Prefill pool, selects the candidate instance with the smallest latency, and then invokes the TTFT prediction model for verification: if the estimated TTFT can still meet the SLO requirements after assigning the request to this instance, the request is allocated immediately; otherwise, it continues to find a suitable instance in the D→P pool. If no instance can meet the TTFT requirements, the instance scheduling mechanism is triggered to allocate resources from the decode side. For decode requests, the scheduler gives priority to having the original prefill instance continue processing (to avoid KV Cache transfer overhead); secondly, it selects the instance with the fewest running tokens in the Decode pool, and checks whether the total number of tokens in its current batch is below the memory capacity upper limit and computing throughput limit determined by pre-analysis, so as to ensure that the new request will not cause TPOT to exceed the standard.

▷ Local Request Scheduler: Each instance adopts a refined queue management strategy internally. KV Cache transfer events are placed in an independent migration queue and processed sequentially in accordance with the FCFS principle; for forward requests, an innovative scheme combining Chunked Prefill [45] and Continuous Batching [8] is adopted: on the premise of ensuring that decode requests are prioritized to enter the running batch, the remaining computing resources are used to process chunked prefill requests in parallel [46].

3.3 Hybrid EPD Disaggregation Scheduler Policy

Challenges of Multi-modal Inference. The inference process of multimodal large language models (MLLMs) [47–52] typically consists of three phases: the image encoding phase (for extracting image features), the prefill phase (for encoding images and text prompts, feeding them into the language model to generate the first output token, and caching intermediate states), and the decode phase (for iteratively generating subsequent tokens based on the cached data). Existing mainstream inference engines, such as vLLM [8], Text-Generation-Inference [53], SGLang [9], and DistServe [13] are all tailored for LLMs, and thus face several challenges in handling inference tasks for MLLMs:

▷ Insufficient Parallelism: For example, the inference of visual models and language models can be executed in parallel, thus improving the utilization of computing resources. However, most existing inference engines [54] adopt a serial strategy, failing to exploit the inter-request parallelism effectively.

▷ Coarse-grained Scheduling: The decode phase is a memory-intensive task, which is suitable for batch processing to improve throughput [55]; the prefill phase is computationally intensive, and it is appropriate to adopt the chunked prefill [45] together with the decode phase to balance latency and throughput [56]. The computation and memory access overhead of the encode phase lies between the two, and it can also benefit from independent scheduling and batch processing. Nevertheless, existing engines process encode and prefill in a combined manner, failing to perform

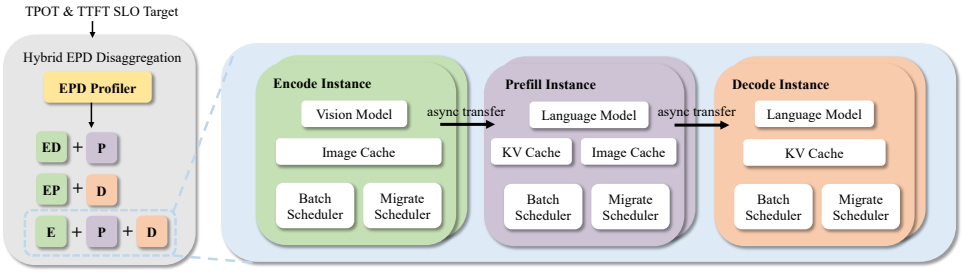

Figure 5: Overview design of Hybrid EPD Disaggregation Policy.

phase-specific batch processing and lacking support for chunked prefill. Coarse-grained scheduling makes it difficult to finely control the execution time.

▷ Disaggregation Strategy: Existing architectures such as DistServe [13] reduce resource interference by decoupling the prefill and decode phases. However, in multimodal inference, encoding and prefill jointly affect TTFT, while prefill and decode jointly determine TPOT. Under different loads, how to select the optimal decoupling strategy remains a challenge [57]. For example, the performance of strategies such as E+P+D, EP+D, and ED+P in different tasks has not yet been evaluated, and in-depth analysis is required to guide system design.

Dual-stream Parallel. As illustrated in Figure 5, we adopt a dual-stream parallel mode, where the visual model and language model are assigned to separate execution streams: the visual stream is dedicated to performing computationally intensive image encoding tasks, while the language stream handles the prefill and decode operations for language generation. By isolating workloads into distinct streams, our system achieves concurrent execution of heterogeneous phases from different requests.

Three-Phase Disaggregation. To address the differences in computation and memory access characteristics among tasks in each phase of multimodal inference, we propose a phase-aware scheduling strategy. Requests are subdivided into three phases within an instance: encode, prefill, and decode. Batch processing and scheduling optimizations are performed for each phase respectively:

▷ Optimized Batch Processing: The maximum batch size for image encoding and the token budget for the language model are set according to the user's SLO. Specifically, during system startup, we use a binary search method to profile the maximum encoding batch size and the model's token budget, ensuring that the execution time of subsequent batch processing tasks in each iteration is less than the TPOT SLO. In each iteration, we (i) first add all running decode requests to the current batch; (ii) then check for any chunked prefill tasks that have been partially computed. If such tasks exist, we add them to the batch; (iii) if there are no chunked prefill tasks, we check for pending encoding tasks and add them if any exist. This approach aims to complete requests in the prefill phase as quickly as possible, reducing their TTFT. New requests' encoding phases are processed only when no requests are in the prefill phase.

▷ Phase-aware Scheduling: To address the difficulty in selecting decoupling strategies for multimodal inference tasks, xLLM proposes the Hybrid Encode-Prefill-Decode Disaggregation architecture, an innovative multi-instance collaborative inference framework. In this architecture, each instance only executes part of the subtasks among the three phases, while the remaining phases are processed by migrating requests to other instances, thereby avoiding resource waste and interference. During runtime, our system automatically selects the optimal disaggregation strategy based on historical request profiling (via *EPD Profiler*) to dynamically balance throughput and latency objectives. Compared with the traditional approach of binding instances to single-phase or full-phase tasks, this architecture significantly improves the overall system processing capability and resource utilization efficiency while meeting SLO requirements.

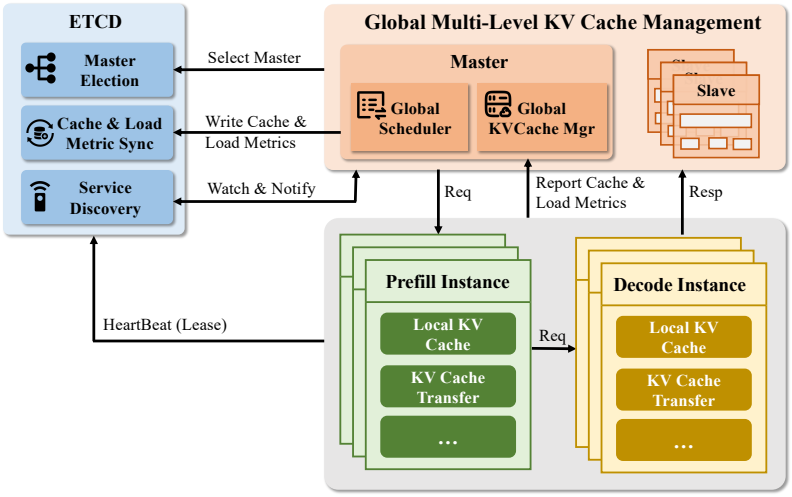

Figure 6: The framework of Global Multi-Level KV Cache Management.

3.4 Global KV Cache Management

During the decode phase of LLMs, subsequent tokens are generated autoregressively one by one. Although the computational cost per step is relatively low, frequent access to the historical KV Cache is required, making memory bandwidth the primary bottleneck. As model size expands and context window grows, the memory consumption of the KV Cache exhibits an exponentially increasing trend. For instance, a context of 128K tokens may consume over 40GB of memory, severely straining the memory resources of single-GPU devices [3].

Although current mainstream optimization solutions like vLLM [8] and FasterTransformer [58] have made significant progress in single-instance environments, many critical issues remain unresolved. In long-context scenarios, the time required for the prefill phase increases dramatically, while the decode phase suffers from intense competition for memory bandwidth. To meet stringent SLO requirements (e.g., TTFT $<$ 2s, TBT $<$ 100ms), one instance often has to reserve excessive resources, instead of leveraging resources in other instances. This significantly restricts the overall cluster resource utilization. To address these challenges, we propose a global multi-level KV Cache management system with a memory-compute integrated architecture, as illustrated in Figure 6.

Distributed Storage and KV Transfer. We adopt the Mooncake Store [23], a KV cache-centric storage engine, as the underlying storage infrastructure for xLLM's KV Cache, along with the Mooncake Transfer Engine as the transmission component. Mooncake Store leverages striping and parallel I/O techniques to fully utilize the aggregated bandwidth of multiple network cards. It provides three persistence strategies—Eager, Lazy, and None—to meet data durability requirements across various scenarios. Additionally, Mooncake Store offers flexible object storage capabilities, supporting multiple replicas and eventual consistency, which effectively mitigates hot-spot access pressure. As the core transmission engine of the system, Mooncake Transfer Engine [23] automatically selects the optimal transmission path based on data location and abstracts low-level complexities through a unified Segment and BatchTransfer interface.

Multi-Level KV Cache Management. At the global level, the system employs ETCD [59] as a metadata service middleware to achieve cluster service registration, load information synchronization, and global cache state management. Each computing instance maintains a local multi-level KV Cache pool (HBM $>$ DRAM $>$ SSD) adhering to the strict consistency rule: "if data resides in HBM, it must also be present in DRAM". Specifically, when local operations involving KV cache (including prefix cache [8]) loading and offloading occur, these operational events are aggregated at regular intervals and transmitted to the xLLM-Service via ETCD heartbeat mechanisms, enabling unified global monitoring and management.

KV Cache-aware Scheduling. In terms of scheduling strategy, the system implements a decision-making mechanism based on KV cache utilization, which operates through three key steps: (1) Prefix Matching Detection: calculating the KV cache reuse rate for each candidate node via prefix matching analysis; (2) Performance Estimation: estimating the expected latency for different nodes according to current load conditions and cache hit rates; (3) Optimal Node Selection: identifying the node with the optimal overall performance for request processing, thereby enabling dynamic offloading and migration of KV cache.

3.5 Fast Fault Recovery Architecture

Current fault handling mechanisms are mainly designed for model training [60–62] and cannot be directly applied to large model inference due to its low-latency requirements. Specifically, existing approaches primarily adopt a checkpoint-then-recovery method [63–65] for fault handling, which periodically stores model data as checkpoints in distributed storage and reloads the most recent checkpoint after a failure occurs [66]. As model parameters increase, the overhead of storage and loading gradually grows. This is still acceptable in training since there are no strict latency requirements [67], but in inference, it may cause all high-priority requests on the failed instance to time out, resulting in severe losses.

To address this issue, we propose an efficient failover architecture specifically for large model inference, with targeted optimizations in two aspects: fast request migration and fast instance recovery. Fast request migration ensures the SLO of high-priority tasks mainly through an efficient kv cache quick recovery strategy, while fast instance recovery achieves low-overhead recovery through efficient masking of computation and communication. Through the above optimization methods, we achieve fast fault recovery, greatly reducing the performance and economic losses caused by faults.

4 xLLM-Engine Designs

4.1 Multi-layer Pipeline Execution Engine

Traditional autoregressive LLM inference relies on single-stream sequential execution. This conventional approach fails to fully exploit the parallelism capabilities of modern hardware, often leading to computational resource underutilization, communication stalls, and cascading blocking delays in heterogeneous computing environments [68, 69]. As illustrated in Figure 7, the system's performance is hindered by three primary sources of inefficiency: (1) *CPU-Accelerator Dependency:* At the framework level, a rigid dependency between the CPU and the accelerator forces the accelerator to remain idle during task scheduling and data processing phases, creating significant "computation bubbles" [68, 3]. (2) *Communication Latency:* In both distributed workloads and complex model layers, communication delays interrupt continuous computation, preventing the full utilization of available hardware resources [69, 70]. (3) *Architectural Bottlenecks:* On certain AI accelerators, the compute-focused (tensor cores) and general-purpose (vector cores) computation units lack a shared high-level cache (e.g., L1 or SRAM). This architectural separation necessitates additional data transfers between them, which introduces latency and leads to the underutilization of the specialized computation units.

To address these challenges, we propose a three-tier asynchronous pipeline parallelism design spanning the framework scheduling layer, the model graph layer, and the operator layer, as shown in Figure 7, with the goal of maximizing hardware efficiency.

Framework-Layer Scheduling-Execution Overlap. In a typical sequential execution procedure, the accelerator remains idle while the CPU performs scheduling to prepare the input data batch for the next computation cycle. This serial dependency creates significant latency and underutilizes the accelerator.

To eliminate this bottleneck, we introduce an asynchronous pipelined scheduling mechanism that decouples CPU scheduling from accelerator execution. The core idea is to overlap these two stages: while the accelerator is executing the forward pass for the current batch, the CPU concurrently assembles the batch and prepares the metadata for the next batch. This parallel workflow effectively hides the latency of CPU-side scheduling and data preparation. The process is as follows: (1) Accelerator Compute: The accelerator is busy executing the forward pass for the current iteration,

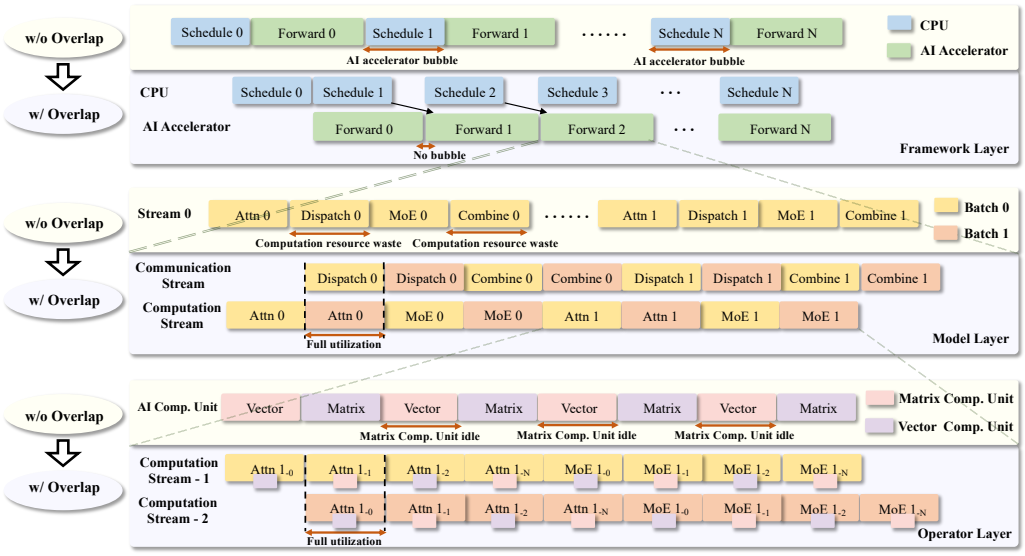

Figure 7: Multi-layer pipeline execution engine.

which will eventually produce output. (2) CPU Schedule: Instead of waiting, the CPU immediately begins scheduling the batch for the next iteration. To do so, it uses a set of placeholder tokens that stand in for the yet-to-be-computed output. This allows all CPU-side batch preparations to occur concurrently with the accelerator's computation. (3) Seamless Transition: Once the accelerator completes the forward pass and the real output is generated, a fast replacement operation swaps the placeholder tokens with the real generated tokens. Since all scheduling is already complete, the accelerator can begin the next forward pass with minimal delay.

By transforming the conventional serial "prepare-then-compute"" workflow into a parallelized pipeline, our method effectively masks scheduling latency behind accelerator computation time. This design eliminates idle execution "bubbles"" in the accelerator timeline, thereby maximizing hardware utilization and enhancing overall system throughput.

Model-Layer Computation-Communication Overlap. Maximizing the overlap between computation and communication is a critical design principle in recent LLM frameworks [3, 71]. This strategy is essential for hiding the significant latency of data transfers and achieving high hardware utilization. However, architectural constraints can make this challenging. For instance, on a typical GPU, compute-focused units (Tensor Cores) are tightly coupled with general-purpose units (CUDA Cores) within a Streaming Multiprocessor (SM). Consequently, when an SM is allocated to a communication-related task, its powerful Tensor Cores often sit idle, leading to wasted compute potential. In contrast, our target accelerator architecture allows for more flexible, independent allocation of its Cube (matrix) and Vector (general-purpose) units. We leverage this flexibility to address the aforementioned challenges by introducing a dual-stream pipeline architecture that uses micro-batch splitting to effectively overlap computation and communication.

Specifically, our architecture consists of a Computation Stream for compute-bound tasks (Attention, ExpertForward, *etc.*) and a Communication Stream for data distribution and collection tasks (MoE Dispatch and Combine). To enable pipelining and maximize overall pipeline throughput, we partition a macro-batch B into n micro-batches [68] $\{b_1, b_2, \cdots, b_n\}$. The two streams asynchronously execute tasks for different micro-batches. On the one hand, our scheduling policy dynamically determines the optimal execution order of the micro-batches. On the other hand, our resource scheduling policy adaptively allocates an appropriate number of AI Cores (Vector Cores and Cube Cores) to the Communication Stream and Computation Stream respectively. Figure 7 illustrates the case of $n = 2$, where the Communication Stream performs the Dispatch operation for micro-batch b_k while the Computation Stream executes the ExpertForward pass for the preceding micro-batch b_{k-1}.

Operator-Layer Matrix-Vector Units Overlap. On heterogeneous AI accelerators, the serial scheduling of matrix and vector computation units often results in significant underutilization, as one class of units remains idle while the other is active. This inefficiency motivates a strategy of operator-level matrix-vector overlap to fully exploit the hardware's parallel capabilities. However, a naive implementation via coarse-grained parallel scheduling, without a systemic resource coordination mechanism, is also problematic. This approach frequently leads to disordered contention for limited compute units, causing resource fragmentation and access conflicts that ultimately degrade overall performance.

To address these challenges, we propose a dynamic resource allocation mechanism for computation units (Cube and Vector Units) based on real-time load monitoring. This mechanism enables a deep pipeline across heterogeneous compute units by dynamically and adaptively assigning the precise type and quantity of resources required for each concurrent operator. By doing so, it mitigates resource contention and ensures that parallel operators execute within highly overlapping time windows, achieving precise computational overlap and maximizing hardware utilization.

We formulate the dynamic resource allocation as an optimization problem. Let $\mathcal{C}$ and $\mathcal{V}$ be the sets of matrix and vector operators, respectively. Let x_i be the number of matrix units (Cube) allocated to the i_{th} matrix operator ($i \in \mathcal{C}$), and y_j be the number of vector units (Vector) allocated to the j_{th} vector operator ($j \in \mathcal{V}$). For simplicity, we assume all operators begin execution simultaneously, without considering data dependencies or communication latency. Based on the known computational workload of each operator, our mechanism seeks to find an optimal resource allocation that minimizes the maximum difference in execution times between any two operators. This objective, which we term the alignment loss ($\mathcal{L}_{align}$), effectively synchronizes the completion time of all parallel kernels. The optimization problem is defined as:

$$\begin{gathered} \operatorname{argmin}_{x_i, y_j} \mathcal{L}_{align} = \max_{i \in \mathcal{C},\, j \in \mathcal{V}} \left| T_i - T_j \right|, \\ T_i = \frac{W_i}{\gamma_{\text{Cube}} \cdot x_i}, \quad T_j = \frac{W_j}{\gamma_{\text{Vector}} \cdot y_j}, \quad \sum_{i \in \mathcal{C}} x_i \le N_{\text{Cube}}, \quad \sum_{j \in \mathcal{V}} y_j \le N_{\text{Vector}}, \end{gathered} \tag{1}$$

where T is the operator execution time, W is its computational workload, γ_{cube} and γ_{vector} are the peak performance per unit, and N_{cube} and N_{vector} are the total available matrix and vector units. The meaning of this optimization objective is to minimize the maximum difference in execution time between any pair of concurrent matrix and vector operators.

4.2 Adaptive Graph Mode

The performance of LLM inference deployment is often impeded by Host-side CPU overhead, particularly when the computation graph is composed of many fine-grained operators [72]. This bottleneck manifests as both significant CPU-Accelerator synchronization latency, measured at $5 \sim 50\mu s$ per invocation from frequent kernel launches, and suboptimal hardware utilization due to idle accelerator cycles between these intermittent operator executions.

Mainstream AI accelerators such as NVIDIA GPUs (with CUDAGraph) [73] and Ascend NPUs (with ACLGraph) [74] employ computation graphs to try to handle above issues and enhance host-side scheduling performance. As illustrated in Figure 8, traditional *Eager Mode* relies on the CPU to submit a multitude of small, intensive tasks, leading to frequent launches of small kernels on the accelerator. In contrast, the *Graph Mode* enables the CPU to submit one large task, after which the accelerator internally executes the small kernels in a streamlined fashion. This method significantly reduces both launch overhead and "accelerator bubbles" (idle cycles). Specifically, the *Graph Mode*, such as ACLGraph [74], comprises two distinct phases: graph capture and graph execution. During the graph capture phase, the entire computation flow is recorded to capture the sequence of kernel calls and their dependencies, including kernel launch parameters. This recorded workflow is then pre-compiled into a replayable directed acyclic graph (DAG) object. It is important to note that during this phase, tasks are merely staged within the model's runtime instance and are not actually executed. In the subsequent graph execution phase, the entire graph is launched via a single CPU call. The accelerator then follows the pre-defined process autonomously, without real-time intervention from the CPU. This effectively consolidates many individual kernel launches into one single graph launch.

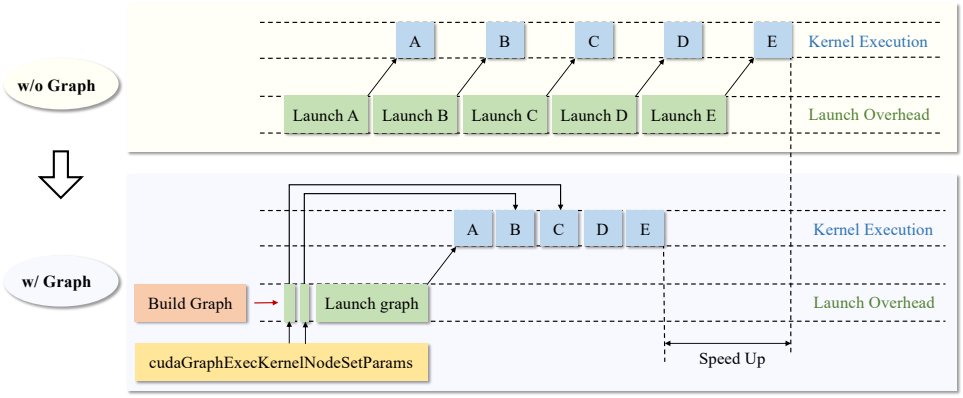

Figure 8: Pipeline comparison between *Eager Mode* and *Graph Mode*.

Building upon this foundation, we further advance the practical implementation of the ACL-Graph [74] and propose our *Adaptive Graph Mode* through addressing key challenges including dynamic shape adaptation, memory reuse conflicts across multiple graphs, and compatibility with custom operators. This enables the pre-compilation of kernel sequences, memory copy operations, and synchronization points into a single computational graph, which is then dispatched to the AI accelerator in one execution. Consequently, our approach significantly reduces kernel launch overhead and minimizes accelerator idle periods, maximizing overall hardware efficiency.

Dynamic Shape Adaptation via Partial Graph and Dimension Parameterization. ACL-Graph [74] fixes kernel parameters and memory sizes during the graph capturing phase. However, in real-world scenarios, LLMs typically process inputs with variable sequence lengths and batch sizes, making this static capturing characteristic difficult to adapt to dynamic input requirements. To address this issue, dimension parameterization can be employed, treating key dynamic dimensions—such as batch size and sequence length—as input parameters to the entire graph, thereby enhancing flexibility. During memory allocation and kernel configuration, these dynamic parameters are used to compute actual required values; for example, the memory size can be calculated using the formula: $alloc_size = batch_size \times seq_len \times hidden_size$. At the graph launch stage, the actual batch size and sequence length are passed as parameters to ensure the graph adapts to varying input dimensions.

Although parameterization can handle variations in dynamic dimensions, certain operator implementations on different hardware may not support dynamic dimension parameterization. To overcome this, we propose the *Partial Graph Mode*: the model is partitioned into modules with simple dynamic shapes (such as FFN and LayerNorm, which only have the num_tokens dimension as dynamic) and modules with complex dynamic shapes (such as Multi-Head Attention, which involves multiple dynamic dimensions like $batch_size$, kv_seq_len, and q_seq_len). Modules with simple dynamic shapes are extracted and compiled for execution using *Partial Graph Mode*, while those with complex dynamic shapes are executed in *Eager mode*. Our *Adaptive Graph Mode* dynamically selects the most appropriate mode above based on the current input shapes. This intelligent selection ensures optimal performance across varying workload conditions.

Table 1 compares the key characteristics of three dynamic shape processing mode. The traditional *Eager Mode* requires no pre-compilation but incurs high scheduling overhead at runtime due to N kernel launches (where N is the number of operators). The *Full Graph Mode*, by fixing shapes, allows single compilation and very low launch overhead, yet its lack of dynamic adaptability limits its applicability. In contrast, the proposed parameterized and multi-caching Partial Graph Mode strikes an optimal balance. It achieves execution performance comparable to that of a full graph while maintaining high flexibility, by trading a manageable number of pre-compilations ($M \ll N_{req}$, where M is the number of cached graphs and N_{req} is the number of actual requests) for the high efficiency of a single graph launch.

Method	Eager Mode	Full Graph Mode	Partial Graph Mode
Compilation Times	0	1	M
Low Launch Overhead	✗	✓	✓
Low Memory Usage	✓	✗	✓/✗
High Flexibility	✓	✗	✓

Table 1: Comparison of different shape handling solutions. Our *Adaptive Graph Mode* dynamically selects the most appropriate mode above based on dynamic shapes.

Efficient and Reusable HBM Memory Pool. During the graph capture process, the specific virtual addresses of input, output, and intermediate tensors are recorded. To prevent illegal memory access, which can occur when the address of an input tensor changes during an actual inference request, we develop a shared HBM memory pool. First, during graph initialization, a sufficiently large, contiguous block of HBM memory is pre-allocated to serve as the graph's memory pool. Subsequently, for internal address management, computation graph intercepts all tensor memory operations and re-describes them using offsets relative to the pool's base address, rather than absolute virtual addresses.

Before the graph is launched, the user-provided input tensor is copied into the HBM memory pool at the offset pre-defined for the graph's input. After graph execution is complete, the data from the output tensor is copied to the user-specified output buffer address. Furthermore, internal tensors within the graph are also managed using fixed offsets within the pool, ensuring safe reuse and efficient memory management. This managed memory pool guarantees that all addresses used internally by the graph are known and safe, which adapts to external address changes with only the overhead of memory copies before and after launch.

Integrating Custom Operators. Integrating performance-critical custom operators, such as PageAttention and AllReduce, into the *Adaptive Graph Mode* presents a unique challenge. The internal implementation of these operators often relies on CPU to perform just-in-time shape calculations and kernel configurations based on runtime inputs. This dynamic behavior conflicts with the pre-compiled nature of computation graph.

To resolve this, we modified the implementation of such operators. The first step is to identify custom operators within the graph that have dynamic shape dependencies. We then refactor these operators to accept shape-related parameters (*e.g.*, dimension sizes or loop counts, which can only be determined at runtime) directly as kernel arguments. This approach avoids hard-coding these values on the host side during the graph capture phase. As a result of this modification, these custom operators can be successfully captured by our computation graph. By leveraging the graph's parameterization mechanism, the required dynamic arguments for these kernels can be derived from the graph's main input parameters and passed along during execution. This method achieves seamless integration of essential custom operators within the *Adaptive Graph Mode* framework.

4.3 Efficient Memory Management

LLM inference deployment faces a critical balance between memory utilization and computational efficiency, particularly in autoregressive generation tasks where efficient KV Cache management has become a key challenge. Traditional solutions fall into two categories: First, contiguous memory allocation approaches that statically pre-allocate memory space based on maximum sequence length before inference, ensuring physical contiguity of KV Cache. While this improves computational efficiency, it results in low memory utilization. Second, PagedAttention [75] approaches that support larger batch sizes through paging mechanisms, but frequent access to block tables sacrifices computational efficiency, and the increased parameters complicate operator development and debugging. To address this challenge, inspired by virtual memory management in operating system field [76, 77], we propose the xTensor memory management scheme, which adopts a "logically contiguous, physically discrete" KV Cache storage structure that resolves the contradiction between

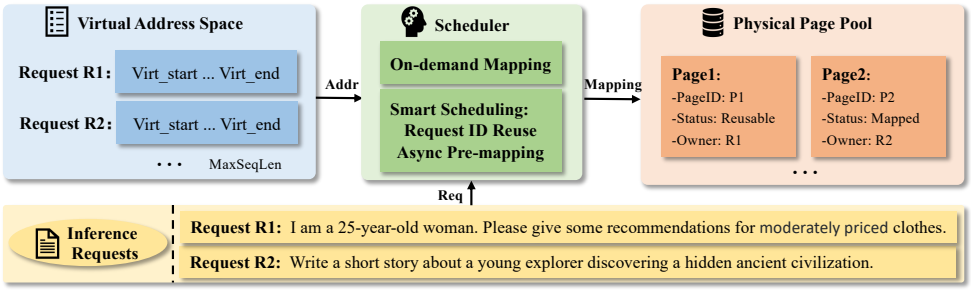

Figure 9: The framework of xTensor memory management.

Features	Contiguous Allocation	Paged Attention	**xTensor** (Ours)
Efficient Memory Usage	✗	✓	✓
Efficient Computation	✓	✗	✓
Large Batch Support	✗	✓	✓
Operator Development Complexity	✓	✗	✓

Table 2: Comparison of memory management strategies.

memory contiguity and dynamic allocation, thereby achieving both high computational efficiency and high memory utilization (as shown in Table 2).

Physical Memory Page Management and Virtual Memory Tensor Management. Figure 9 illustrates the xTensor memory management framework. During service initialization, based on the available memory size for KV Cache, a large number of fixed-size discrete physical memory pages are pre-allocated. Each physical page maintains a triple state $\langle PageID, Status, OwnerSession \rangle$, where $PageID$ represents the page identifier, $OwnerSession$ indicates the service owning the page, and $Status \in \{Free, Allocated, Mapped, Reusable\}$ represents states of free, allocated, mapped, and reusable to dynamically track physical page usage. Subsequently, each inference request is pre-allocated with a logically contiguous virtual address space with an address range equal to $MaxSeqLen$, where this virtual address space is not actually associated with physical pages during allocation. This decoupled design provides operators with a virtual view of KV Cache stored in contiguous memory, thereby masking the discrete nature of underlying physical pages [78, 79].

On-demand Memory Mapping. During actual allocation, the scheduler dynamically maps physical memory pages on-demand based on the actual sequence length of requests. When a sequence generates new tokens and KV Cache needs expansion, the scheduler retrieves one or more free pages from the pre-allocated physical page pool and maps these physical pages to the next available contiguous address location in the request's virtual address space. Since physical memory is gradually mapped as sequences grow, short sequences only require a small amount of physical memory, thus avoiding the memory waste of contiguous allocation strategies that still require reserving space according to maximum sequence length for short sequences.

After memory mapping is completed, kernel access to virtual addresses can automatically locate the corresponding physical page $phypage_{idx}$ and $offset$:

$$\begin{aligned} phypage_{idx} &= \left\lfloor \frac{virt_addr - virt_start}{page_size} \right\rfloor, \\ offset &= (virt_addr - virt_start) \bmod page_size, \end{aligned} \tag{2}$$

where $virt_addr$ and $virt_start$ represent the current virtual address and starting virtual address respectively, and $page_size$ represents the physical page size.

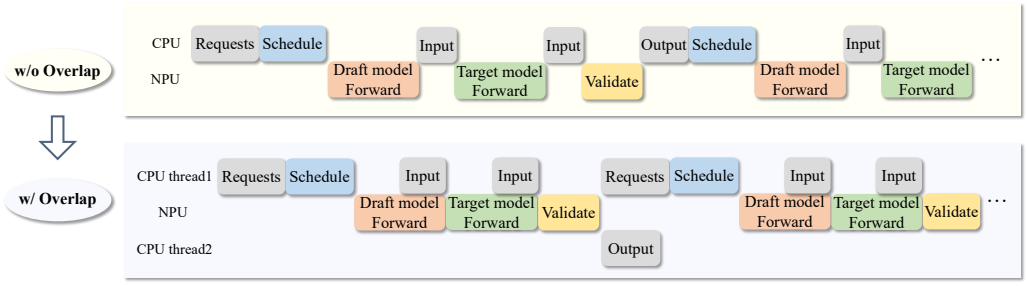

Figure 10: Comparison between original and our optimized speculative decoding.

Low Overhead Allocation. If virtual address to physical page mapping is immediately released upon request completion, new requests require remapping physical pages, but the $Unmap$ operations on accelerators incur significant overhead. Therefore, under high load conditions, frequent Map/$Unmap$ operations become performance bottlenecks, especially for numerous short-term concurrent requests. We adopt request ID reuse and asynchronous pre-mapping designs to reduce latency from Map/$Unmap$ operations.

- **Physical Page Reuse.** Upon request completion, physical pages are not immediately released but marked as Reusable. When new requests arrive, if their required KV Cache size matches some Reusable physical page set, that page set is remapped to the new request's virtual address space. This saves expensive Map and $Unmap$ operations through fast virtual address remapping, particularly suitable for scenarios with concentrated request length distributions.
- **Asynchronous Pre-mapping.** During current token decoding, the next token's required physical pages are asynchronously predicted and mapped. Since new token writes to KV Cache occur after current token decoding computation, this design can partially hide physical page mapping operations, significantly reducing page mapping latency.

Operator Adaptation. The decoupled design of xTensor's physical memory pages and virtual contiguous memory requires the adaptation of existing operators. On one hand, to accommodate KV Cache contiguity in virtual address space, operators no longer require $block_table$ parameter input. Whether for attention operators or $write_kvcache$ operators responsible for writing KV Cache during Prefill and Decode phases, only the starting virtual address and related offsets need to be passed in, with the system automatically associating virtual addresses to corresponding physical pages during operation. On the other hand, accelerators lack native contiguous KV FlashMLA [80] operators and only support PagedFlashMLA [80] operators optimized for paging. Therefore, by reconstructing the PagedMLAttention operator in the accelerator operator library, removing Block Table-related logic such as block table queries and cross-page boundary judgments, and adding functionality for direct computation based on input virtual addresses, we implement FlashMLA operators supporting contiguous virtual address input on accelerators.

4.4 Algorithm Optimizations

4.4.1 Optimized Speculative Decoding

Traditional autoregressive inference requires LLMs to generate tokens sequentially one by one, resulting in high computational latency and limited throughput. Speculative decoding technology theoretically breaks through this performance bottleneck through a paradigm of parallelly predicting candidate token sequences and quickly verifying them [81, 82, 26]. However, in distributed deployment environments, this technology faces some core challenges: *First*, synchronous scheduling between CPUs and accelerators in traditional multi-step inference frameworks results in insufficient utilization of computing resources, with accelerators often remaining idle while waiting for data preparation and processing. *Second*, existing attention mechanisms are not optimized for the characteristics of speculative inference, causing a large amount of redundant data movement. To address these challenges, xLLM proposes a systematic optimization scheme based on existing frameworks.

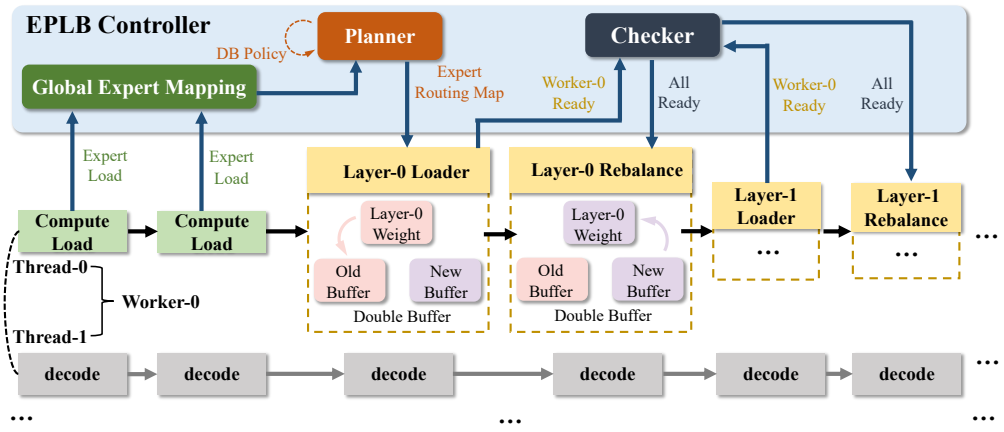

Figure 11: Overview design of EPLB.

Asynchronous Decoding. Inspired by [83], xLLM implements a lightweight asynchronous framework. For timing overlap optimization, while the accelerator executes the main model inference for the current batch, the CPU processes the output decoding of the previous batch and the input preparation for the next batch in parallel—thereby minimizing the idle time of the CPU and accelerator as much as possible.

MLA Optimization. xLLM focuses on improving the MLA [84, 3] computation process. Based on the characteristic that speculative inference needs to process multiple tokens simultaneously on a single sequence, we conducted in-depth optimizations on the self-attention computation in MLA. Specifically, when speculatively inferring m tokens, the self-attention computation of MLA involves product operations between m+1 Q matrices and the same K matrix. By reconstructing the computation process and optimizing the tiling strategy, we effectively reduced the data movement overhead of Q/K matrices. The main optimization measures include:

▷ Optimization of K matrix loading times: By adjusting the L1 cache allocation scheme to enable parallel loading of multiple Q matrices, and adopting a sliding window-based K matrix loading method that allows consecutive rows of the K matrix to multiply with multiple Q matrices, the number of K matrix loading operations is significantly reduced.

▷ Q matrix cache residency mechanism: Since there are m+1 Q matrices in speculative inference scenarios, the time to move Q matrices to L1 accounts for a larger proportion of the matrix multiplication process. xLLM redesign the computing scheme to prevent softmax-V product operations from overwriting Q matrices in the L1 cache, enabling Q matrices to remain in the cache and significantly reducing the overhead of repeated data movement, thereby effectively improving the utilization of the tensor core's arithmetic logic units.

4.4.2 Dynamic EP Load Balance

With the large-scale application of MoE models [85–88] in production environments, their efficient inference capability relies on a expert routing mechanism, which allocates input tokens to different experts for computation [3, 18, 89]. However, in practical deployment, due to the distribution characteristics of input data and the influence of the model's own structure, there may be significant differences in the number of tokens received by different experts [90, 91]. This imbalance leads to low computing resource utilization: some devices are overloaded due to processing too many tokens, while others remain idle, affecting the overall inference efficiency.

To optimize resource utilization, the industry has proposed the Expert Redundancy strategy, which means replicating hot experts and deploying replicas on multiple devices to distribute computing loads. Currently, DeepSeek [3] adopts two load balancing strategies: group-limited load balance and global load balance, which are optimized respectively for the characteristics of the prefill and decode phases. Adjustments to expert redundancy (such as adding/deleting replicas) require ad-

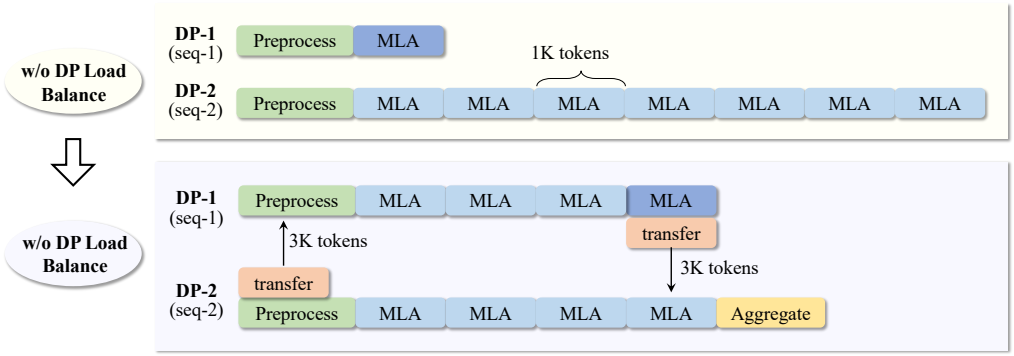

Figure 12: Inter-DP group load migration at MLA block granularity.

ditional memory and may affect inference latency due to weight migration. How to achieve such adjustments efficiently and smoothly is a major challenge. We have made some adaptive improvements based on DeepSeek, realizing dynamic EP load balance.

Expert Load Statistics. When the Router distributes tokens, it records the load status of each expert in real time and returns the statistical results through the model output. Each Worker asynchronously starts a thread to periodically aggregate expert loads and report them to the Controller of the Master. The Controller calculates a new routing table based on the load data and then distributes the updated routing table to each Worker.

Double Buffer Mechanism for Weight Update. In general, each Worker starts an asynchronous thread to update the weights of single-layer experts during each decoding process. Specifically, after a Device completes the preparation of new weights, it proactively sends a readiness notification to the Controller. The Controller then verifies the weight readiness status of all Worker nodes to ensure global consistency before broadcasting an update instruction, upon which each Worker executes the weight update immediately. Here, we adopt a Double Buffer mechanism, meaning that the old and new expert weights are stored in two separate buffers respectively. The new expert weights are preloaded in the spare memory space, and after the preloading is completed, the address switching is performed to realize the unperceived update of experts.

4.4.3 Hierarchical DP Load Balance

In typical MoE model architectures like DeepSeek [3], the MoE layers use expert parallelism (EP), while the attention layers use data parallel (DP). This model requires all DP groups to synchronously complete their attention calculations in a single inference step before initiating the MoE all-to-all dispatch operation. This synchronization barrier means the total time for the attention phase is determined by the slowest DP group (the "straggler"). Faster DP groups cannot immediately proceed to the next stage after finishing their tasks; instead, they are forced into an idle state, waiting for the straggler to complete [92]. This waiting directly translates into wasted computational resources and an increase in overall inference latency.

In practical scenarios, due to the dynamic and unpredictable nature of inference requests, the load within different DP groups is often difficult to balance. Particularly in the decoding phase with large-scale DP (e.g., 80 groups), the load difference between DP groups can reach tens of thousands of tokens, causing fast DP groups to wait for slow ones and wasting approximately 5 milliseconds of delay [93]. Experimental data shows that although the difference in the number of requests processed between DP groups may be as small as four, the corresponding difference in KV Cache token count during the decoding phase can be as high as 20,000. The actual computational workload is directly related to the total number of tokens the system needs to process, as this determines the memory footprint of the KV Cache and the scale of matrix operations in the attention mechanism. This further establishes DP load balancing as a critical factor in determining overall system efficiency.

Current mainstream frameworks like vLLM [8] and SGLang [9] use a simple static round-robin scheduling strategy. Once a request is assigned, its subsequent computations are fixed to a specific

DP group, making it unable to adapt to dynamic load changes. Furthermore, at the hardware level, the implementation of operators like the MLA on certain accelerators employs a "one request per tensor compute core" partitioning strategy. This can lead to idle compute cores within the same DP group due to differences in request lengths.

To address these challenges, xLLM proposes a hierarchical "defense-in-depth" strategy to tackle DP load imbalance issues across different time scales and granularities. The first layer is preventative, KV Cache-aware request scheduling; the second layer performs macroscopic correction through inter-DP group load balancing; and the third layer carries out microscopic correction via intra-DP group load balancing. This layered design enables the system to flexibly address the root causes of various performance degradations, thereby building a robust and efficient inference service.

Layer 1: KV Cache-Aware Scheduling. xLLM's first-layer strategy implements request load distribution through KV Cache-aware scheduling. This mechanism moves beyond simple round-robin methods. When a new request arrives, the scheduler comprehensively checks the status of all DP groups, paying special attention to the remaining KV Cache capacity in each. It then preferentially assigns the new request to the group with the most available space. By balancing the total token load and its memory footprint at the system level over the long term, this strategy prevents the formation of severe load imbalances, thereby achieving intelligent resource allocation.

Layer 2: Reactive Inter-DP Group Workload Migration. xLLM's second-layer strategy achieves reactive balancing through workload migration between DP groups. During the decoding process, the varying prompt and KV Cache lengths of selected requests cause different computation latencies among DP groups. To counter this, xLLM's central scheduler evaluates the current computational load of each DP group during every inference round. If a significant imbalance is detected, it initiates a workload migration process, moving tasks from overloaded to under-loaded groups. The scheduler also determines the migration granularity – whether to move an entire batch, a single sequence, or a partial MLA block of a sequence.

Figure 12 illustrates this process at the MLA block granularity. First, xLLM dispatches the input tokens for the migration to both the source and destination DP groups. Then, as all groups execute the MLA Preprocess operation, the request's KV Cache is transferred asynchronously, overlapping communication with computation. Next, all groups begin the attention calculation. The underloaded group prioritizes the migrated attention task, allowing it to immediately send the resulting token back to the source group upon completion while concurrently processing its own native attention operations, further overlapping overhead. Finally, all DP groups use an aggregation operator to gather the external computation results.

Layer 3: Fine-Grained Kernel-Level Optimization. xLLM's third-layer strategy achieves fine-grained optimization through kernel-level migration within a DP group. This optimization is performed inside the matrix computation kernels of a single DP group. On one hand, during scheduling, it reorders requests based on their load, replacing the original compute core's round-robin allocation strategy. This aims to keep the total number of computation tokens assigned to each matrix computation unit as consistent as possible. On the other hand, for requests with extremely long sequences, it explicitly splits their computation sequence, migrating parts of the long-sequence request's computation to be calculated with other short-sequence computation units. Through this fine-grained request splitting, it directly resolves the issue of idle compute cores caused by load imbalance within the DP group.

4.5 Generative Recommendation

Recent advancements in generative models have spurred significant interest in generative recommendation [31, 94–98]. Beyond enhancing the retrieval and ranking stages of traditional multi-stage pipelines [98, 94], single-stage generative recommendation frameworks directly generate a candidate item list in an auto-regressive manner [31]. These frameworks usually utilize beam search decoding to directly produce diverse recommendation results, and xLLM implements extensive optimizations for these single-stage frameworks. As shown in Figure 13, in the generative recommendation scenario, xLLM is dedicated to overlapping host and device operations as much as possible to improve overall execution efficiency. When a request arrives, xLLM preemptively prepares the information required during the forward process on the CPU side. After the preparation is completed,

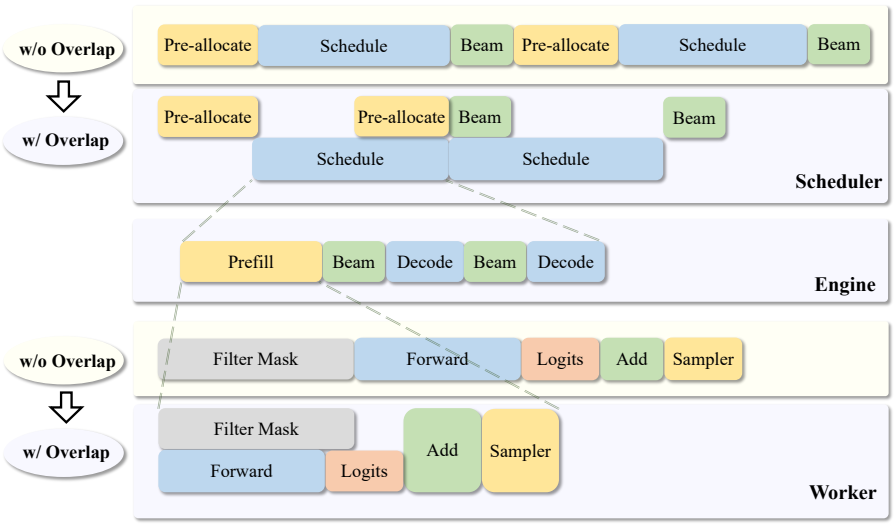

Figure 13: Overview design of generative recommendation process.

relevant tasks are handed over to the engine for processing. The Engine executes three forward passes in one go. During this process, the intermediate beam search is a host operation, which by its nature cannot be overlapped with device operations. To optimize the processing pipeline, xLLM internally employs a multi-micro-batch, multi-stream approach. During the Worker's execution, the CPU operation for generating the filter mask is overlapped with the device operation for logits computation. Through an addition operation, a masked logits is generated before the sampler, thereby achieving data filtering and improving the accuracy and effectiveness of the recommendation results.

4.5.1 Host-side Optimization

In scenarios with large $beam_width$ and top_k parameters, the significant increase in the number of candidate sequences results in substantial sorting and filtering operations on the host side. This shifts the computational bottleneck of the beam search algorithm from the AI accelerator to the CPU, ultimately leading to a severe CPU-bound issue. The following outlines xLLM's efforts to optimize the beam search process in generative recommendation scenario.

Beam Search Optimization. In many fields such as natural language processing, beam search optimization is an efficient algorithm widely used in sequence generation tasks [99]. When processing a large number of candidate sequences, one of the core operations of beam search is to select $beam_width$ sequences from numerous candidates. This process is essentially a partial sorting operation, with the unique characteristic that it only needs to identify the top $beam_width$ elements without fully sorting all candidate sequences, thereby significantly reducing computational complexity. In another key step of beam search, generating $beam_width \times top_k$ candidate sequences from the existing $beam_width$ sequences, there exists an important property: log_probs of each sequence are arranged in descending order. Leveraging this property, an optimized early termination mechanism can be adopted, where computations are halted prematurely if log_probs does not meet specific criteria, further enhancing computational efficiency. The specific operational procedure is as follows:

First, the existing $beam_width$ sequences are accessed in order. For each accessed sequence, we create a small min-heap of size $beam_width$, which is used to dynamically maintain the set of locally optimal elements currently selected. Next, the subsequent sequences are traversed. During this process, if the subsequent log_probs of a sequence is smaller than the top element of the min-heap, it implies that, based on the current filtering criteria, the subsequent elements of this sequence cannot enter the current optimal set. At this point, the filtering operation for the current sequence can be terminated directly, and the next existing sequence processed. Conversely, if the subsequent log_probs is larger than the top element of the min-heap, the element is inserted into the min-heap,

and the heap structure is adjusted according to the properties of the min-heap to maintain its order. After the traversal of all relevant sequences is completed, the top elements are sequentially extracted from the min-heap. These elements, in the order of extraction, form the $beam_width$ candidate sequences sorted in descending order. Through this procedure, the approach ensures the selection of high-quality candidate sequences while significantly reducing unnecessary computational overhead, thereby improving the operational efficiency of the beam search algorithm in practical applications.

Resource Reuse and Pre-allocation. During the beam search process, the $beam_width$ is predetermined and fixed for each forward pass of the model, which implies that the computational resources required per forward propagation remains relatively constant. However, an excessively large $beam_width$ can lead to significant wastage of both CPU computational and memory resources. To effectively mitigate this issue, xLLM incorporates a carefully designed resource reuse strategy. Specifically, during the generation of new candidate sequences, the system reuses resources previously occupied by older sequences without allocating new space for each candidate. This approach avoids the overhead associated with frequently creating new data structures. Based on the final search results, the system then updates the storage areas for the old sequences with the content of the newly generated ones upon completion of the beam search algorithm. By doing so, xLLM not only reduces memory usage but also minimizes the additional overhead on the CPU for resource management and allocation, significantly improving the efficiency of computational resource usage.

4.5.2 Device-side Optimization

Valid Item Filtering. In typical single-stage generative recommendation frameworks, the valid item filtering mechanism plays a crucial role. For example, OneRec [31] framework uses an ordered combination of three token IDs to uniquely represent a valid product item ID. However, due to the vast number of possible token ID combinations, not all of them correspond to actual and valid items [100, 101]. To ensure that the results generated by the model are all valid product items, the system generates a valid mask asynchronously during the forward pass of the model. This mask is based on a pre-constructed vocabulary of valid items, which is then element-wise added to the logits output by the model. Through this clever design, the logits corresponding to invalid token IDs are adjusted, ensuring that these invalid token IDs are almost never selected in subsequent calculations. This effectively filters out invalid token IDs, thereby guaranteeing the validity and accuracy of the final recommendation results.

5 Evaluations

In §5.1, we evaluate the full implementation of our xLLM framework against several baseline inference systems, specifically vLLM-Ascend[1](v0.10.rc1) and MindIE[2](v2.1.rc1), on Ascend 910B/910C [18] instances across a range of scenarios. xLLM, MindIE, and vLLM-Ascend refer to the default deployments on Ascend 910B. Additionally, we denote the deployments of xLLM, MindIE and vLLM-Ascend on Ascend 910C as xLLM‡, MindIE‡ and vLLM-Ascend‡, respectively. The testing scenarios are organized into multiple categories reflecting diverse online serving applications, such as the JingYan AI chatbot, customer service assistants, merchant assistants, product understanding and marketing recommendation systems. Additionally, in §5.2, we conduct a detailed ablation study to assess the individual contributions of each optimized module.

5.1 Main Results

This section benchmarks xLLM against mainstream inference frameworks to demonstrate its superior inference efficiency across diverse models, including Qwen2/3-series [102, 87] and Deepseek [3] models, and datasets. §5.1.1 details a fair comparison using the ShareGPT[3] dataset. To ensure an equitable comparison across all LLM inference frameworks, **the key feature of our experimental setup is that the input and output sequence lengths are fixed, while the request**

[1] https://github.com/vllm-project/vllm-ascend

[2] https://www.hiascend.com/en/software/mindie

[3] https://huggingface.co/datasets/anon8231489123/ShareGPT_Vicuna_unfiltered/blob/main/ShareGPT_V3_unfiltered_cleaned_split.json

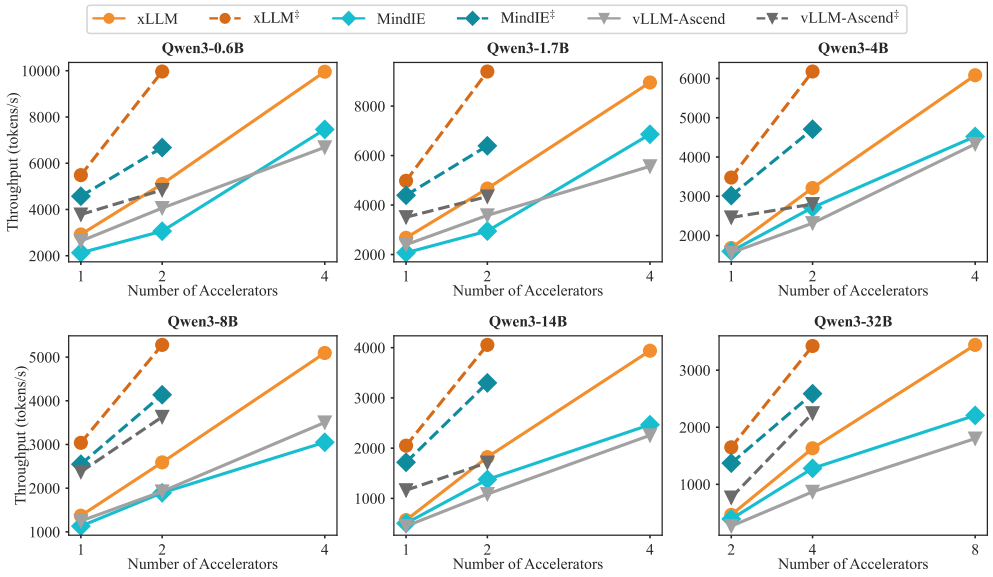

Figure 14: Throughput comparison of LLM inference frameworks evaluated on Qwen3-series models using the ShareGPT dataset, under the constraint of *TPOT=50ms* and *input/output length=2048*.

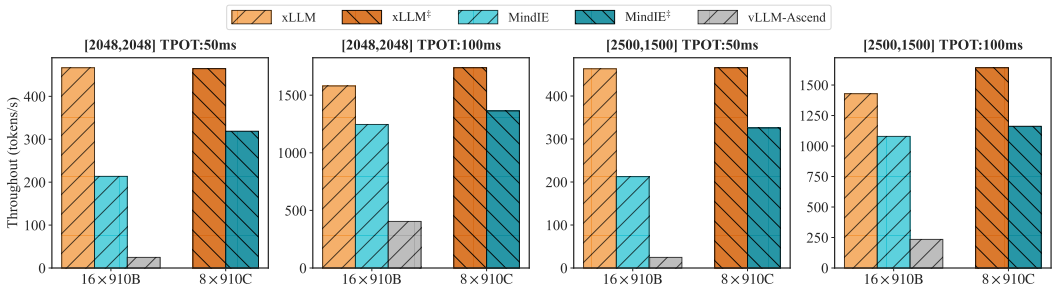

Figure 15: Throughput comparison of LLM inference frameworks using DeepSeek-R1 on the ShareGPT dataset constrained by given TPOT and input/output length, where *[2500, 1500]* means *input length=2500* and *output length=1500*. vLLM-Ascend on the 910C is excluded from the comparison, as its performance with Deepseek-R1 fails to meet the required TPOT threshold.

rate is dynamically adjusted to match the target SLO (e.g., TPOT) threshold for each framework. We also evaluate this setup under different node configurations, including both single-node and multi-node setups with PD disaggregation. In §5.1.2, we evaluate xLLM on various real-world business scenarios from JD.com, where it is currently deployed, showcasing its performance under practical deployment conditions.

5.1.1 Benchmarking Performance

Qwen3-series. As shown in Figure 14, we comprehensively compares the throughput performance of four inference frameworks across the Qwen3-series (from 0.6B to 32B parameters) on the benchmark. All tests are conducted under uniform configuration with input/output lengths set to 2048 tokens and a TOPT constraint of 50 ms. The experimental results demonstrate that while all evaluated frameworks show improved throughput with additional accelerators, xLLM and its Ascend 910C implementation (xLLM‡) consistently deliver superior performance, confirming near-linear strong scalability across various model sizes. Specifically, xLLM achieves throughput improvements of up to 1.9× and 1.7× compared to vLLM-Ascend and MindIE, respectively. Similarly, xLLM‡ outperforms vLLM-Ascend‡ and MindIE‡ by up to 2.2× and 1.5×, respectively. Further-

Method	Prompt Length	Output Length	Throughput (tokens/s)	Request Rate (req/s)
MindIE	2048	2048	8476.44	4.14
xLLM	2048	2048	**11351.58**	**5.54**

Table 3: Comparison of DeepSeek-R1 with PD disaggregation on the ShareGPT dataset constrained by *TPOT=100ms*.

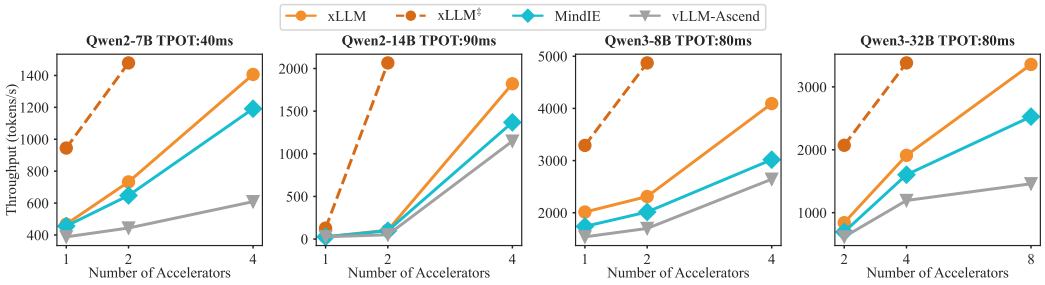

Figure 16: Throughtput comparison of Qwen2-series and Qwen3-series models with various inference frameworks in the JingYan scenario.

more, xLLM‡ demonstrates steady performance improvements over the Ascend 910B-based xLLM in most scenarios, validating the software stack's effective utilization of the new hardware.

DeepSeek-R1. Figure 15 presents the throughput performance of various inference frameworks for the DeepSeek-R1 model on the benchmark, using 16 accelerators for Ascend 910B and 8 accelerators for Ascend 910C, respectively. The results demonstrate that the proposed xLLM framework achieves exceptional throughput on the Ascend 910 series. Quantitatively, xLLM on Ascend 910B delivers an average throughput improvement of approximately 1.7× over MindIE and a significant 12× enhancement over vLLM-Ascend. Furthermore, xLLM‡ achieves an average throughput increase of approximately 1.4× compared to MindIE‡.

PD Disaggregation Settings. Table 3 benchmarks the inference performance of the MindIE and xLLM frameworks on the DeepSeek-R1 model using a PD disaggregation architecture. Under identical conditions with TPOT controlled at 100ms for 2048-length inputs/outputs, xLLM achieves approximately 34% higher throughput (11,351.58 vs. 8,476.44 tokens/s) and request rate (5.54 vs. 4.14 req/s), marking a significant efficiency improvement.

5.1.2 Business Serving Scenarios

JingYan. JingYan is an AI shopping assistant designed to help users discover new products, find inspiration, and get answers to their questions. The dataset for JingYan, consequently, consists of conversational logs between the model and its users, capturing these rich interactions. As illustrated in Figure 16, we systematically evaluate the inference throughput of four frameworks for serving the Qwen2-series and Qwen3-series model in the JingYan scenario. The results demonstrate that both xLLM and xLLM‡ maintain superior throughput and exhibit better scaling efficiency across all model sizes compared to MindIE and vLLM-Ascend. For instance, when serving the Qwen3-8B model with 4 accelerators, xLLM delivers a throughput approximately 1.6 times that of vLLM-Ascend and significantly surpasses MindIE. The robust performance of xLLM on the 910B, and its enhanced results on the 910C hardware, highlight its effective adaptation to successive hardware generations. As shown in Table 4, a similar trend is observed for the DeepSeek-V3 model, where xLLM achieves a throughput that is over 9 times greater than vLLM-Ascend and surpasses MindIE by 36%.

Customer Service. The Customer Service dataset comprises the interactive dialogues between customers and support agents. Figure 17 details the performance differences among inference frame-

Method	Prompt Length	Output Length	Throughput (tokens/s)	Request Rate (req/s)
vLLM-Ascend	6800	400	21.17	0.11
MindIE	6800	400	144.40	0.67
xLLM	6800	400	**196.45**	**0.89**

Table 4: Comparison of Deepseek-V3 model with various frameworks in the JingYan scenario constrained by *TPOT=80ms*.

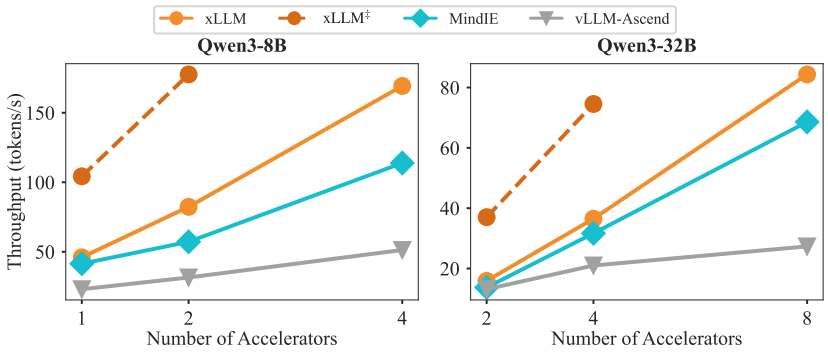

Figure 17: Throughtput comparison of Qwen3-series models with various inference frameworks in the customer service scenario constrained by *End-to-End latency(E2E)=10s*.

works for the Qwen-8B and Qwen-32B models in the customer service scenario. The results highlight that our xLLM, particularly the xLLM‡ running on Ascend 910C, provide significantly better throughput across all tested configurations. For instance, with Qwen3-32B on 8 accelerators, the throughput of xLLM is 3.1 and 1.2 times greater than that of vLLM-Ascend and MindIE, respectively. It is important to note that the vLLM-Ascend framework shows a clear scaling bottleneck as the number of accelerators increases, whereas xLLM maintains near-linear efficiency scaling. This validates the high efficiency and superiority of the xLLM framework in managing distributed inference for large-scale models.

Merchant Assistant. Table 18 benchmarks the throughput of various inference frameworks on three tasks (i.e., search terms, arrangement, intent recognition) within the merchant assistant scenario. The proposed xLLM framework achieves better or comparable performance to MindIE and demonstrates a significant lead over vLLM-Ascend. Specifically, for the search terms task with four accelerator cards, xLLM delivers 34% higher throughput than MindIE and roughly 3.4× that of vLLM-Ascend.

Product Understanding. For the product understanding scenario, the throughput comparison of the Qwen2-7B model with several frameworks is shown in Table 5. The experimental results indicate that xLLM outperforms MindIE and vLLM-Ascend by an average of 25% and 56%, respectively, across different accelerator card counts. Moreover, the superiority of xLLM scales with the number of cards, demonstrating its effective utilization of large-scale parallel computing resources and thereby offering a robust solution for high-performance LLM inference.

Generative Recommendation. As illustrated in Figure 19, the evaluation results on the Qwen-8B model demonstrate that xLLM consistently achieves lower mean end-to-end latency than MindIE across various request rates and beam widths, except under very low load condition. Notably, the performance advantage of xLLM becomes increasingly pronounced as the beam width (from 4 to 128) and the request rate escalate. For instance, under the most challenging scenario with a beam width of 128 and a request rate of 8, xLLM reduces latency by approximately 23% relative to MindIE. This significant improvement validates that our xLLM's host-side and device-side optimizations effectively alleviate the computational bottlenecks in generative recommendation tasks, markedly enhancing inference efficiency and scalability under heavy loads.

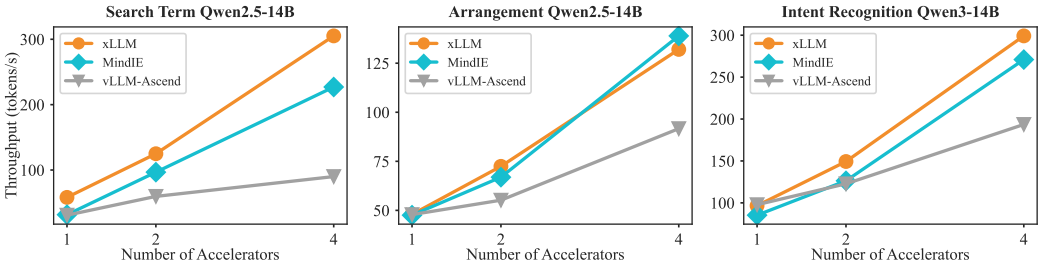

Figure 18: Throughtput comparison of Qwen-series models with various inference frameworks in the merchant assistant scenario constrained by *End-to-End latency(E2E)=1s*.

Method	Prompt Length	Output Length	Throughput (tokens/s)		
			#accelerator=1	#accelerator=2	#accelerator=4
vLLM-Ascend	1200	40	795.77	874.97	1272.52
MindIE	1200	40	944.81	1051.44	1693.45
xLLM	1200	40	**1001.91**	**1323.90**	**2425.13**

Table 5: Throughtput comparison of Qwen2-7B model with various inference frameworks in the product understanding scenario.

5.2 Ablation Study

Impact of MTP. As shown in Figure 20, under the configuration of 1500 input length and 2500 output length for the DeepSeek-R1 model, enabling Multi-Token Prediction (MTP) technology significantly optimizes inference performance. As max concurrency increases, the MTP-enabled version consistently exhibits lower TPOT compared to the baseline, indicating reduced generation latency. Meanwhile, its throughput is markedly higher than the non-MTP version, with particularly notable advantages beyond 32 concurrent requests. This demonstrates that MTP effectively enhances computational efficiency and system throughput under high concurrency conditions.

Impact of Dynamic PD Disaggregation Scheduler Policy. We evaluate our proposed SLO-aware Dynamic PD Disaggregation Policy against the Minimal Load and Round Robin strategies, as illustrated in Figure 21. On the Azure Code dataset characterized significant bursty traffic, our SLO-aware policy achieves a request serving rate 1.67 times that of the Minimal Load strategy. Meanwhile, relative to the Round Robin strategy, the Minimal Load strategy improves the SLO attainment by up to 4.3%. For the Azure Conversation dataset with stable input/output length variations, our SLO-aware policy results in a 1.1 times higher request serving rate compared to the Minimal Load strategy. Although the Minimal Load strategy performs similarly to Round Robin, it still enhances the SLO attainment by up to 2.4%. These results indicate that minimal-load scheduling is closer to the optimal scheduling strategy than round-robin approach, while our adaptive instance scheduling delivers the best overall performance.

Impact of Hybrid EPD Disaggregation Scheduler Policy. Figure 22 demonstrates the effectiveness of the proposed Hybrid EPD Disaggregation Policy on the TextCaps dataset, specifically in controlling TPOT and improving the SLO attainment rate. Under the configuration of 8 general-purpose inference instances, the removal of the hybrid EPD disaggregation method results in a drop in goodput from 9.5 req/s to 7.2 req/s, and a subsequent additional removal of stage-level scheduling policy further decreases the goodput to 5.1 req/s. This indicates that a well-designed disaggregation strategy can effectively mitigate inter-stage interference, while our stage-level scheduling policy contributes to finer control over the execution time of each batch. The integration of both components significantly enhances the overall performance and stability of the system, particularly under high-concurrency scenarios.

Impact of Online-Offline Co-location Scheduler Policy. As shown in Figure 23, we evaluated three scheduling strategies, namely the baseline P/D, online priority and our proposed Online-Offline

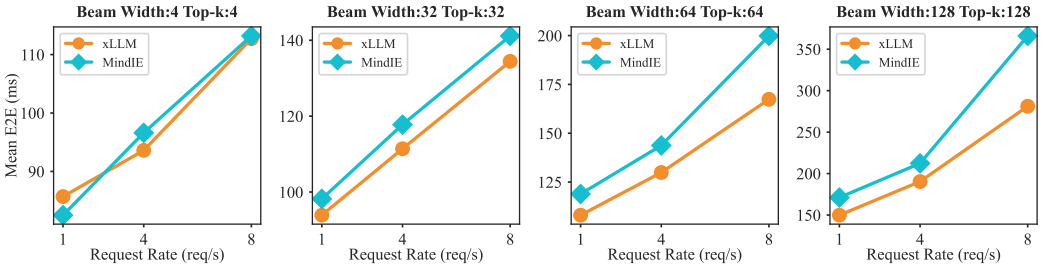

Figure 19: Comparison of mean End-to-End latency(E2E) with various inference frameworks in the generative recommendation scenario. Since vLLM-Ascend does not support *beam width>10*, the corresponding results are not plotted in the figure. Even with *beam width=4* and *request rate=1*, its mean E2E far exceeds that of our framework.

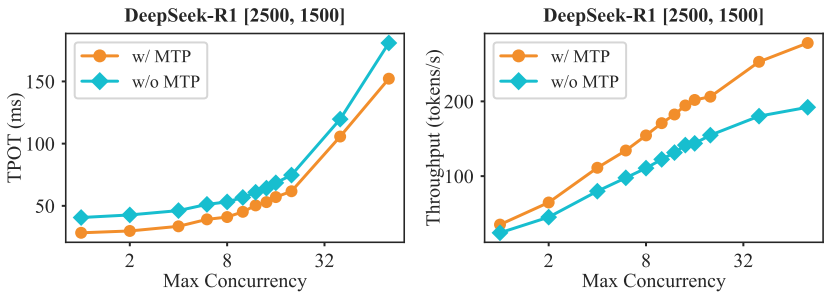

Figure 20: Impact of MTP on the concurrent performance of DeepSeek-R1 model.

Co-location Scheduler Policy (denoted as xLLM-OOC), to assess the maximum achievable throughput for offline requests without violating the SLO of online requests. The green shaded region in the figure indicates the sustainable range of offline request throughput that remains within the acceptable online SLO violation threshold. When the offline query-per-second (QPS) exceeds a certain level, both the baseline P/D and online priority strategies lead to a sharp increase in the online SLO violation rate, indicating interference caused by the offline workload. In contrast, xLLM-OOC maintains stable SLO compliance even as offline QPS continues to rise. On our proprietary dataset, xLLM-OOC achieves a throughput that is three times higher than the other two methods. Furthermore, it demonstrates improvements of 75% and 17% over online priority and baseline P/D, respectively, on the Azure Code dataset.

Impact of Multi-layer Pipeline Execution. As evidenced by the results in Table 6, our proposed asynchronous scheduling mechanism delivers consistent throughput improvements across all evaluated model scales. The most substantial relative gain of 17.4% is observed for the 1.5B parameter model, highlighting the method's particular efficacy for smaller architectures where scheduling overhead constitutes a larger portion of total computation time. While relative improvements moderate for larger models (reaching 0.6% for 7B, 3.7% for 14B, and 6.6% for 32B), all configurations exhibit statistically significant absolute gains. These results robustly validate that our method successfully masks scheduling latency and eliminates computational bubbles, through leveraging placeholder tokens to decouple and overlap CPU scheduling with NPU execution.

We further assess the effectiveness of the proposed dual-stream architecture for the DeepSeek-R1 model in Table 7. Experimental results from a single decoder layer show that the total communication time increases to 12.4ms in dual-stream mode, up from 9.3ms in single-stream mode. However, the computation-communication overlap mechanism successfully hides 80% of the communication time, which brings the exposed communication time down to just 2.5ms, saving 6.8ms per layer. Despite introducing a computational overhead of 4ms for each layer, the dual-stream strategy yields a net performance gain of 172.0ms across the entire 61-layer model, clearly illustrating the capability of our scheduling strategy in real-world workloads.

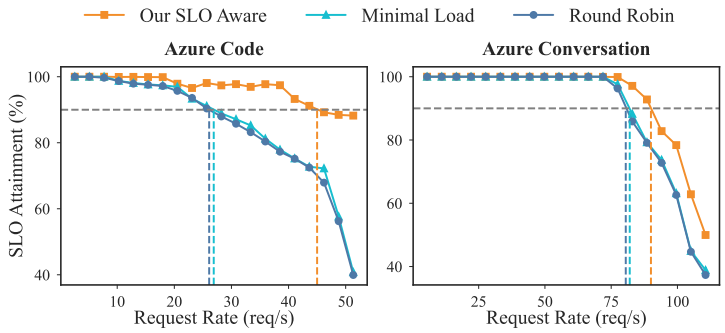

Figure 21: Performance of Dynamic PD Disaggregation Policy with different scheduling strategies.

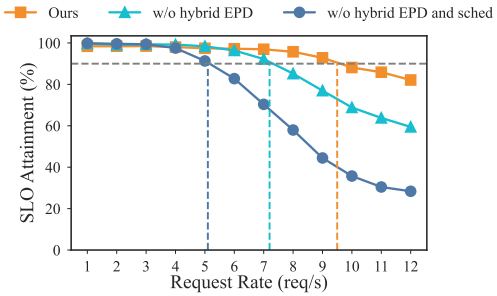

Figure 22: Impact of Hybrid EPD Disaggregation Scheduler Policy.

Impact of Adaptive Graph Mode. To validate the effectiveness of the Adaptive Graph Mode optimization technique, we conduct controlled experiments on the Qwen3-1.7B and Qwen3-4B models. As shown in Table 8, with both the prompt and output lengths set to 2048 tokens, enabling Adaptive Graph Mode result in significant performance gains for both models. The throughput of Qwen3-1.7B increases from 2385.58 to 3038.88 tokens/s (a 27.4% improvement), while its mean TPOT decreases by 22.0%. Correspondingly, Qwen3-4B achieved an 8.5% increase in throughput and an 8.8% reduction in latency. These results robustly demonstrate the effectiveness of Adaptive Graph Mode as a general-purpose inference acceleration technique, with more pronounced optimization effects observed on the model with a smaller parameter size.

Impact of Hierarchical DP Load Balancing. Our proposed hierarchical DP load balancing scheme is projected to increase total throughput by 5%. The kernel-level optimization yields the most significant latency savings; for example, for an ultra-long 32k-token request, reordering and splitting can reduce a single core's computational load from 32k to 1.3k tokens, saving approximately 800 microseconds. In contrast, the latency savings from inter-DP group migration are more modest. Even after balancing a 20k-token difference, the total time saved over 61 Transformer layers is only about 600 microseconds. This indicates that the greatest performance bottleneck and optimization potential lie within the computation units themselves.

6 Future Work

Although proposed xLLM framework has demonstrated potential in enhancing LLM inference efficiency and reducing operational cost, achieving truly efficient and inclusive intelligent computing infrastructure requires deeper collaborative innovation across **Hardware**, **Model**, and **Application** Layers. Our future research will advance xLLM from a high-performance *Inference Engine* toward a comprehensive *Operating System for AI* that supports next-generation intelligent applications. We outline our planned efforts in three key directions:

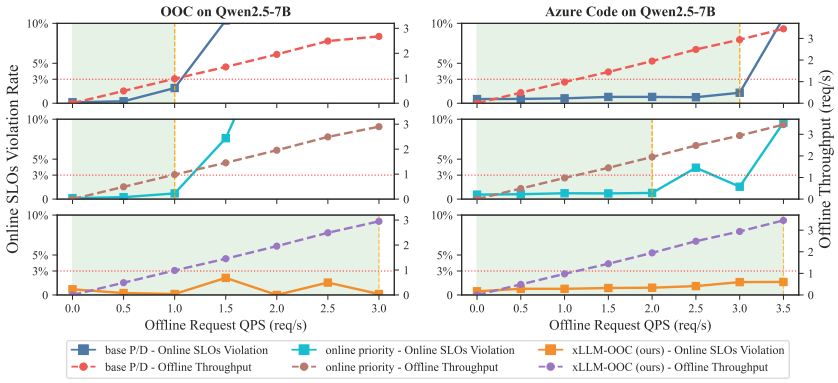

Figure 23: Impact of our Online-Offline Co-location Scheduler Policy.

Model	Prompt Length	Output Length	Async Scheduling	Throughput (tokens/s)
DS-Distill-Qwen-1.5B	1000	1000	×	8709.90
	1000	1000	✓	**10223.15**
DS-Distill-Qwen-7B	1000	1000	×	3183.68
	1000	1000	✓	**3201.83**
DS-Distill-Qwen-14B	1000	1000	×	1472.22
	1000	1000	✓	**1527.23**
DS-Distill-Qwen-32B	1000	1000	×	1415.20
	1000	1000	✓	**1508.76**

Table 6: Impact of asynchronous scheduling mechanism in Multi-layer Pipeline Execution.

6.1 Fostering an Open and Diverse Hardware Ecosystem

Current AI infrastructure often suffers from tight coupling with specific hardware architectures, introducing computational stability risks and limiting efficient deployment in heterogeneous environments such as edge computing. To address this, the first pillar aims to cultivate an open and diverse hardware ecosystem through the following initiatives:

Unified Hardware Abstraction Layer. We will develop a high-performance, hardware-agnostic runtime abstraction layer that encapsulates instruction sets and memory architectures across computational units—from domestic cloud chips to edge-side accelerators. This layer will provide unified operator interfaces and memory management APIs, enabling seamless migration and efficient execution across heterogeneous hardware without code modifications, thereby significantly reducing integration barriers for emerging hardware.

Software-Hardware Co-Design and Ecosystem Synergy. We will collaborate with hardware partners to define more efficient and open interface standards. This co-design approach will not only drive hardware innovation from the software perspective but also help establish a self-sustaining and competitive computational supply ecosystem, ultimately providing users with optimized choices across cost, performance, and security considerations.

6.2 Cultivating a Vibrant and Responsive Model Ecosystem

The system's core value derives from its supported model diversity and integration efficiency. Our future efforts will focus on building an inclusive and agile model ecosystem through:

Multi-Scenario Support. We will extend the platform's optimization and deployment capabilities beyond large language models to systematically support various generative AI scenarios, including generative recommendation, text-to-image, and text-to-video generation. We will optimize execu-

Metric	Single-Stream (ms)	Dual-Stream (ms)
Total Communication Time	9.3	12.4
Overlapped Communication Ratio	-	80%
Exposed Communication Time	9.3	2.5
Total Computation Time	13.0	17.0
Reduced Time per Layer	-	2.8
Total Reduced Time (61 layers)	-	172.0

Table 7: Communication and computation overheads in a single decoder layer of DeepSeek-R1 using Multi-layer Pipeline Execution.

Model	Prompt Length	Output Length	Adaptive Graph Mode	Throughput (tokens/s)	Mean TPOT (ms)
Qwen3-1.7B	2048	2048	×	2385.58	39.27
	2048	2048	✓	**3038.88**	**30.63**
Qwen3-4B	2048	2048	×	1539.93	55.44
	2048	2048	✓	**1671.39**	**50.58**

Table 8: Impact of Adaptive Graph Mode.

tion engines, request scheduling, and memory management specifically for different workloads to ensure optimal performance across diverse applications.

"Zero-Day" Model Integration. To accommodate rapidly evolving model architectures, we will implement a unified framework combining model graph representation, an extensible operator library, and automated compilation optimization. This will enable rapid "zero-day" integration of newly released models, reducing deployment cycles from weeks to hours.

6.3 Evolving into an AI-Native Application Framework

To democratize AI adoption and accelerate value delivery, we will evolve the system from an inference engine into a full-stack AI-native application framework by:

Framework-Native AI Middleware. We will design high-level, framework-native APIs and abstractions that package complex distributed inference, multi-model orchestration, and stateful session management capabilities into out-of-the-box middleware services. This will enable application developers to build sophisticated AI applications (e.g., multimodal AI agents) without managing underlying infrastructure complexities.

Rapid Application Integration and Deployment. Building upon this AI-native framework, we will deliver a comprehensive toolchain — including encapsulated SDKs, application templates, and integrated CI/CD pipelines — to streamline development and deployment processes. Our goal is to enable application teams to integrate and deploy AI services within hours rather than weeks, significantly enhancing business innovation agility and fully bridging the "last mile" from model development to value creation.

7 Conclusion

We introduce **xLLM**, an intelligent and efficient LLM inference framework, featuring a service-engine decoupled architecture. The framework consists of two main components: (1) **xLLM-Service**, a versatile service layer designed for efficient instance and cluster management as well as request scheduling. It incorporates unified elastic scheduling for co-located online and offline requests to maximize cluster utilization, a workload-adaptive PD disaggregation architecture for SLO-aware dynamic instance scheduling, a novel Encode-Prefill-Decode (EPD) disaggregation mechanism for multimodal requests, a global KV Cache manager for efficient memory management including KV Cache upload and offload and a distributed fault-tolerance design to ensure high availability. (2) **xLLM-Engine**, a high-performance inference engine optimized for accelerating LLM

inference across various AI accelerators. xLLM-Engine employs full-stack multi-layer execution pipeline optimizations through asynchronizing CPU-side scheduling and AI accelerator-side model forwarding to minimize computational bubbles, utilizing dual-stream parallelism of micro-batches to overlap computation with all-to-all communication, and further overlapping various AI computation units at the operator level. xLLM-Engine also implements an adaptive graph mode which pre-compiles kernel sequences, memory operations, and synchronization into a single computation graph to drastically reduce launch overhead and accelerator idle time. Additionally, it adopts a "logically contiguous, physically discrete" KV Cache storage strategy via proposed xTensor Memory Management, which resolves the tension between memory contiguity and dynamic allocation. To further boost hardware utilization, xLLM-Engine integrates algorithmic enhancements such as asynchronous pipelined adaptive speculative decoding, KV cache-aware scheduling, reactive inter-DP group workload migration for dynamic load balancing, and dynamic MoE load balancing based on real-time expert workload statistics and transparent weight updates. We have further extended xLLM to emerging generative recommendation scenarios, improving both recommendation accuracy and efficiency.

Extensive experiments demonstrate that xLLM achieves a consistent improvement compared to leading inference systems such as MindIE and vLLM-Ascend, evaluated across mainstream Qwen-series and Deepseek-series models as well as public and real-world industrial datasets. In particular, xLLM outperforms MindIE by up to 1.7$\times$ and vLLM-Ascend by up to 2.2$\times$ in throughput. Comprehensive ablation studies further validate the effectiveness of key components, including the proposed scheduling modules, multi-layer execution pipeline, optimized model tensor parallelism, adaptive graph mode, and others.

By releasing the xLLM framework as an open-source project, we intend to stimulate further innovation in developing robust, enterprise-scale inference solutions, optimizing performance on a diverse range of AI accelerators, and creating tightly integrated service and engine architectures for next-generation AI applications.

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